III КОНФЕРЕНЦИЯ FPGA РАЗРАБОТЧИКОВ

FPGA-Systems 2021.2

Доступно в записи на Youtube

Конференция в Москве

Конференция в Санкт-Петербурге

Приходи на следующую конференцию

fpga-systems.ru/meet

Поддержи мероприятие

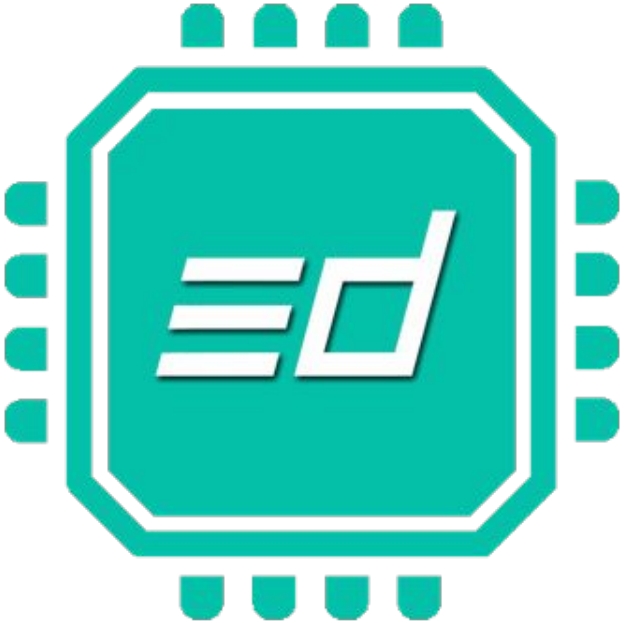
Способ 1

Способ 2

YET ANOTHER FPGA MEZZANINE

DMITRY MURZINOV

TELEGRAM CHANNEL



t.me/embedoka

FPGASIC BOOK

idoka.ru/book

WHO AM I

DMITRY MURZINOV

- ★ Ms Degree in Radio Engineering
- ★ 17 years FPGA experience
- ★ 13 years ASIC experience
- ★ 7 years Signal Processing
- ★ 3 years in HW Cryptography
- ★ 2 years in ML implementation on HW

DISCLAIMER

- User of DevBoard Point of View
- The time-limited presentation
- A quite prepared audience
- The Final|Draft specs doesn’t exist at the moment

AGENDA

EXISTING SOLUTIONS (HISTORY)

THE MAIN ISSUES OF CURRENT SOLUTIONS

WHY NEXT GEN MEZZANINE? (PROS ANS CONS)

USECASES

ROADMAP

CONCLUSION

EXISTING SOLUTIONS

HSMC (High Speed Mezzanine Card) (Altera)

VITA57 2008: FMC HPC/LPC, FMC+ (FPGA Mezzanine Card)

PMOD (Digilent)

ZMOD (Digilent, based on SYGYZY by Opal Kelly)

VHDCI (Vmod from Digilent)

*MicroMod (NGFF based with modified mounting)

EXISTING SOLUTIONS

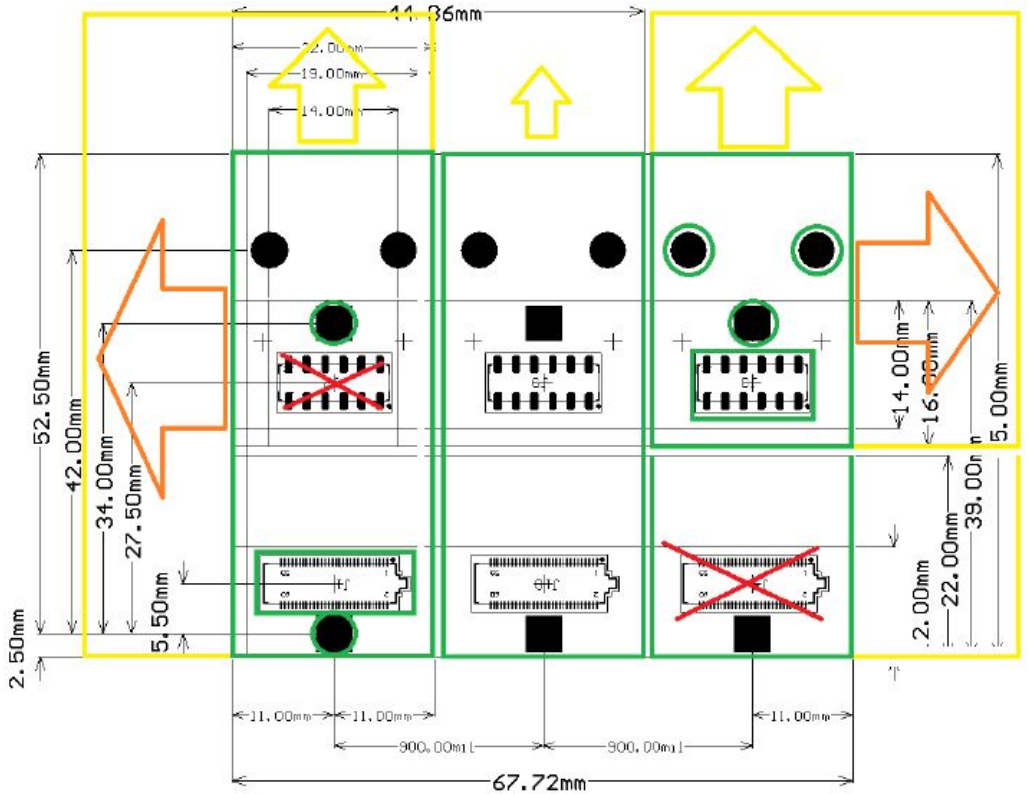
VHDCI (Vmod from Digilent)

EXISTING SOLUTIONS

CRUVI

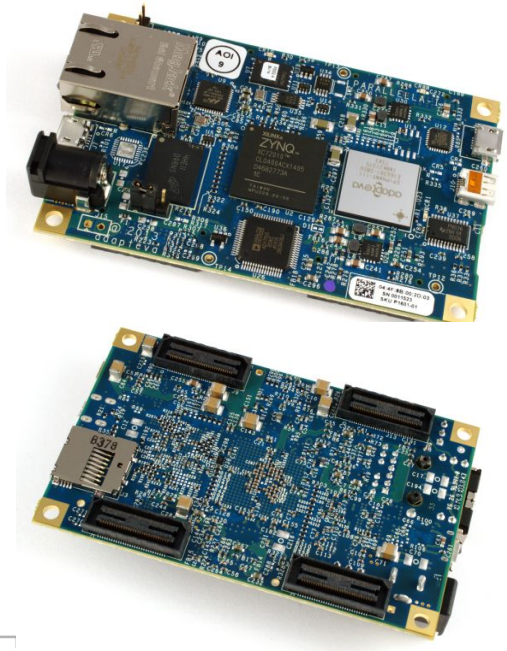
Working Group Members:

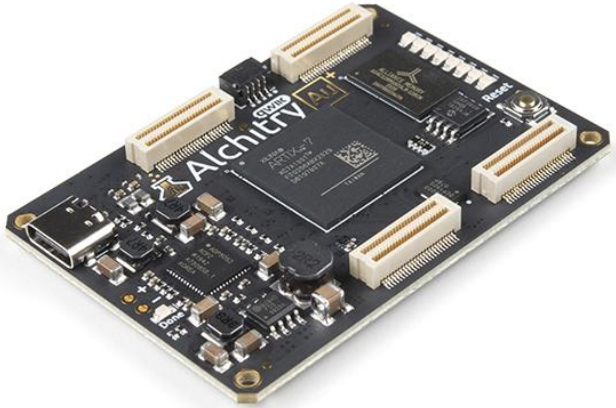
- Flinders University
- FOSSi Foundation
- MicroFPGA UG
- Symbiotic EDA
- Trenz Electronic GmbH
- Samtec

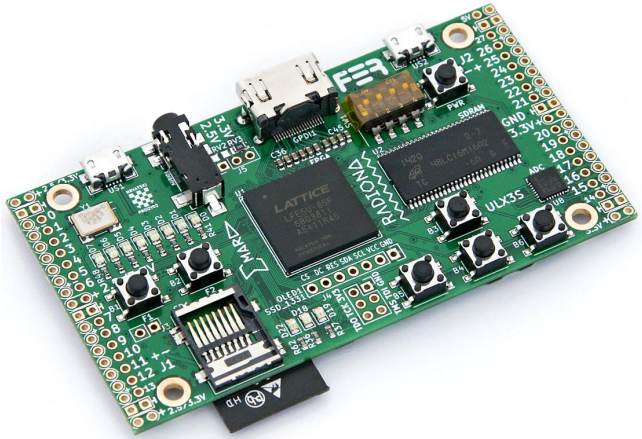


EXISTING SOLUTIONS

Some crowdfunding projects:

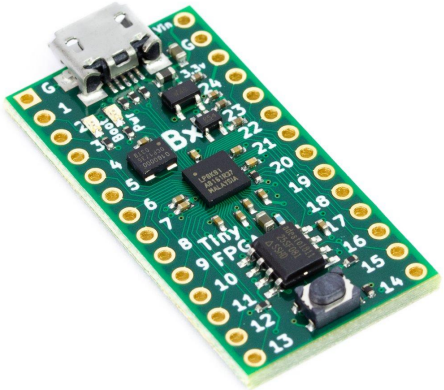


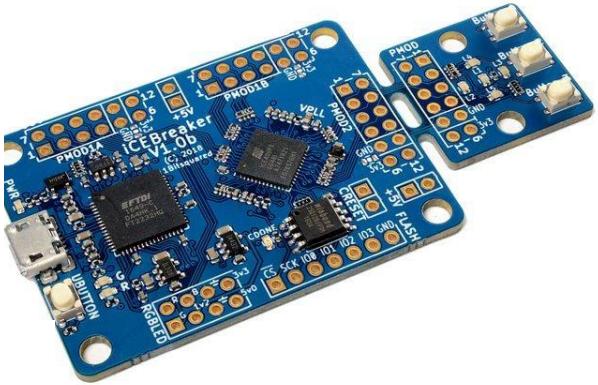


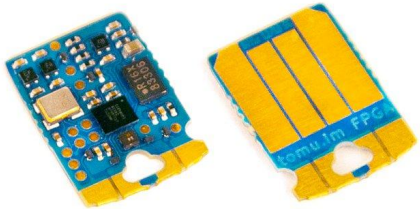


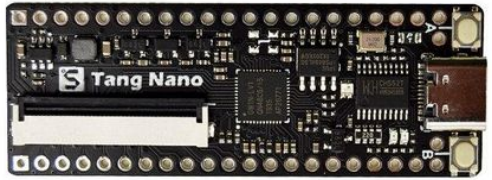
EXISTING SOLUTIONS

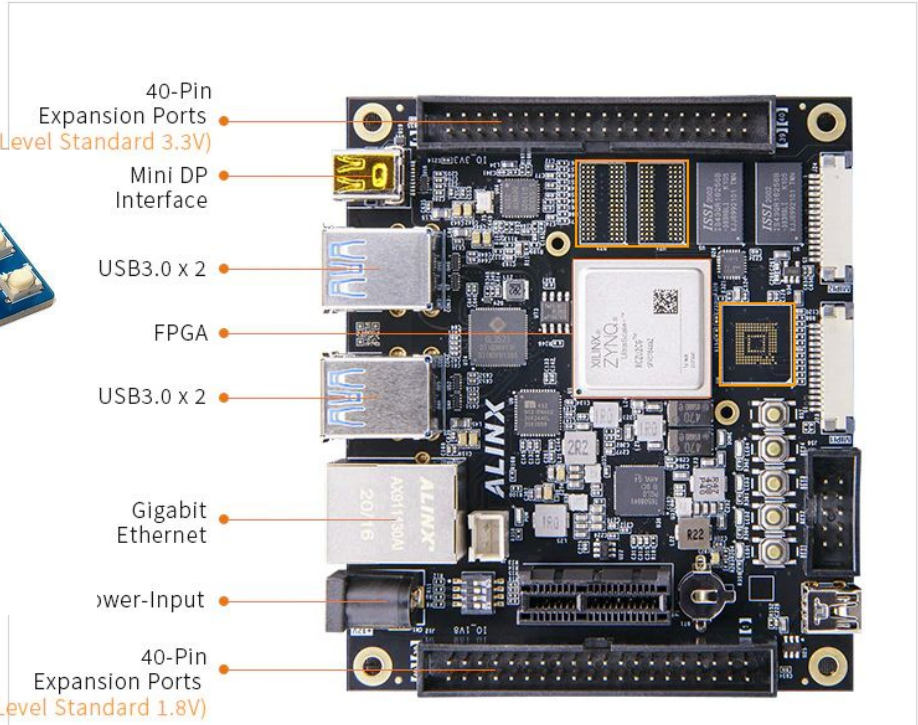
Random FPGA-projects from Web:











Note: AXU2CGA Memory is 2 Pieces of DDR4, a total of 1GB, No EMMC FLASH

FMC'S ISSUES

1. Connectors` lead time (time-to-deployment)

5767056-1

Enlarge

Images are for reference only
See Product Specifications

Mouser No:	571-5767056-1
Mfr. No:	5767056-1
Mfr.:	TE Connectivity / AMP
Customer No:	Customer No
Description:	Board to Board & Mezzanine Connectors .025 PLG 2X019P VRT
Datasheet:	5767056-1 Datasheet
ECAD Model:	PCB Symbol, Footprint & 3D Model

Download the free Library Loader to convert this file for your ECAD Tool. Learn more about the ECAD Model.

Compare Product

Add To Project | Add Notes

In Stock: 260

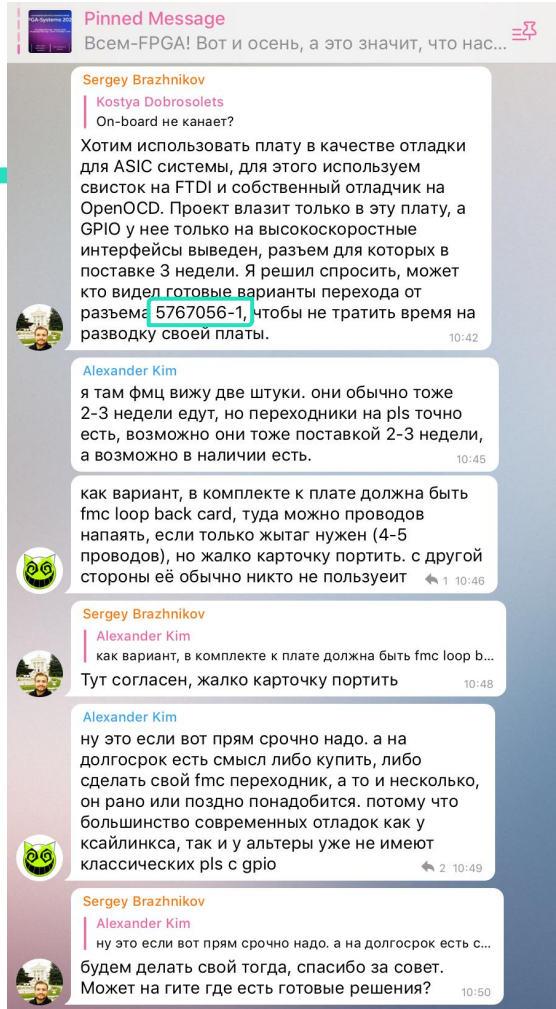
Stock:	260 Can Dispatch Immediately
Factory Lead Time:	11 Weeks

Minimum: 1 Multiples: 1

Enter Quantity: Buy

Pricing (EUR)

Qty.	Unit Price	Ext. Price
1	20,14 €	20,14 €
10	18,18 €	181,80 €
21	17,41 €	365,61 €
42	16,33 €	685,86 €
105	15,78 €	1.656,90 €
252	14,91 €	3.757,32 €
504	14,47 €	7.292,88 €

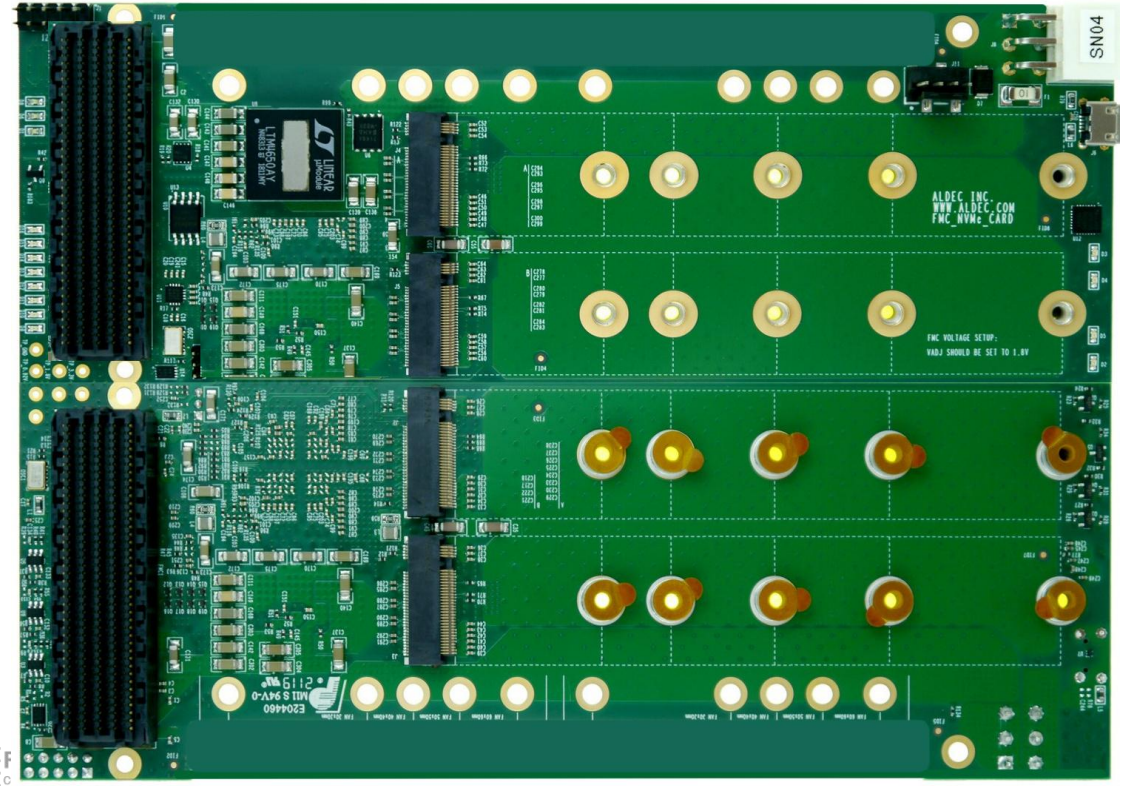


FMC'S ISSUES

2. Daughter boards cost (a quite expensive):

- Connector's cost
- PCB cost:
  - Should be Multilayer (to routing 40x10 pins' array)
  - Dimension (defined by FMC standard)
- Soldering procedure:
  - BGA-like footprint (do not try at home)

MEET NEXT GEN FPGA MEZZANINE



DOKARD

DOKARD'S MOTIVATION

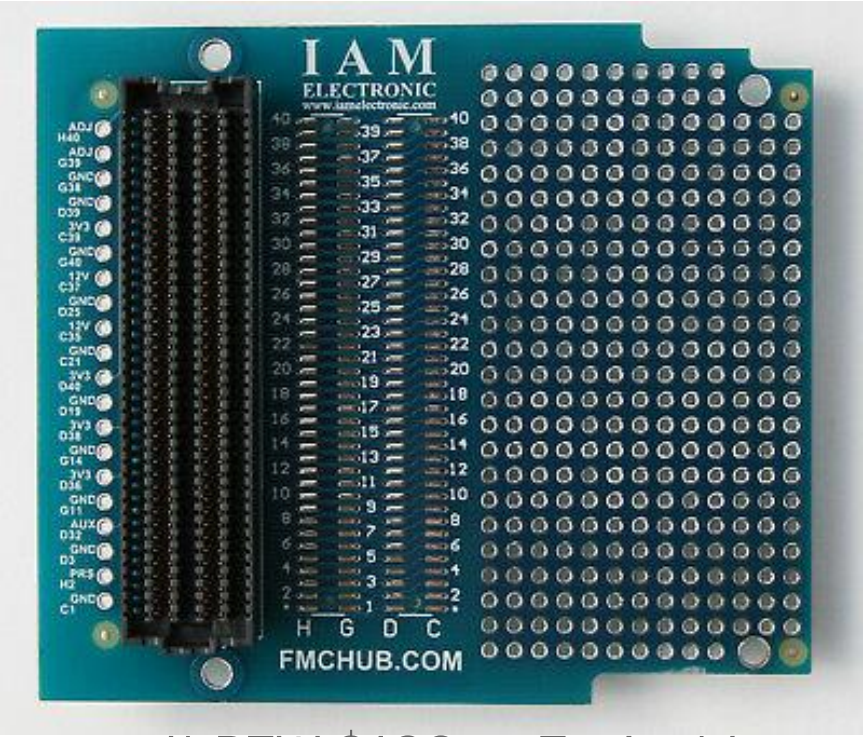
- ❏ Nearly Zero Waste
- ❏ Rapid time-to-deploy
- ❏ Daughter boards as cheap as possible (e.g. "no cost" connectors by design)
- ❏ Flexibility in terms of purpose (usecases)
- ❏ Powerful Plug&Play capabilities

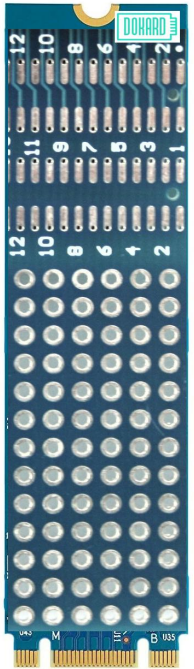
See next slides for detail

NEARLY ZERO WASTE

- No plastic for connectors (on daughter-board side)
- Minimal PCB size started from 22mm x 30mm
  (enough for most “single IC” daughter-boards)
- Reuse and Aftermarket
  (hopefully DOKARD boards will be widely accessibility)

RAPID TIME-TO-DEPLOY





/* BTW $120 on Tindie */

BOARD'S COST

(DOKARD-based) Daughter boards might be as cheap as possible.

Decided to move some components on MainBoard:

- ❑ Connector and ESD clamps
- ❑ DC/DC for Vadj generating
- ❑ Source clocks synthesizing capabilities
- ❑ LEDs, DIP switches
- ❑ Terminals
- ❑ USB-hubs/USB-connectors
- ❑ Signal level translators (see slide UNDER CONSIDERATION)

USECASES

1. MVP of FPGA projects (before releasing HW rev.1)
2. ASIC prototyping (HW in loop)
3. PoC (Proof of Concept) of SBC/SoC projects
    - Including small production batches
4. HW Electronics Enthusiasts

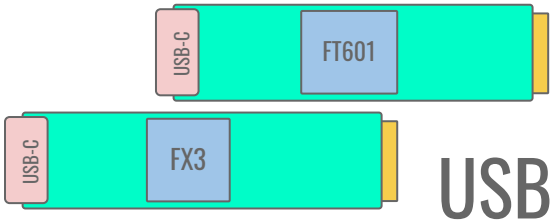
MVP OF FPGA PROJECTS

MVP of FPGA projects (e.g. before releasing HW rev.1)

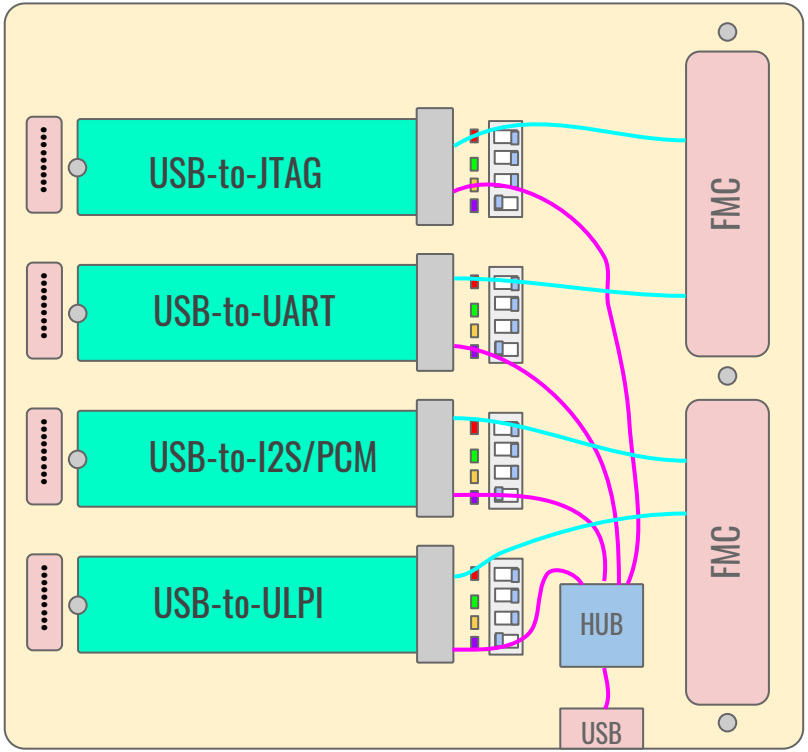
- Early build on real HW-environment and bring-up procedures
- Production of tiny batches for rapid time-to-market
  (it might be faster and cheaper in comparison with FMC-based design)

ASIC PROTOTYPING

- Hardware-in-the-Loop capabilities
- Included all advantages of previous item



USB3.0 SS



PoC OF SBC/SoC PROJECTS

Proof of Concept and Small Batches for SBC/SoC-based projects

- Rapid time-to-market and small batches production
- End-user features configurability

DIY ELECTRONICS ENTHUSIASTS

PLUG & PLAY CAPABILITIES

T.B.D. (See ROADMAP slide)

DOKARD DISADVANTAGES

1. 0.8mm PCB thickness required
2. Highly recommend ENIG finishing for PCB
3. Low mechanical hardness (PCB strength)
4. Poor availability of DOKARD boards (hopefully temporary)

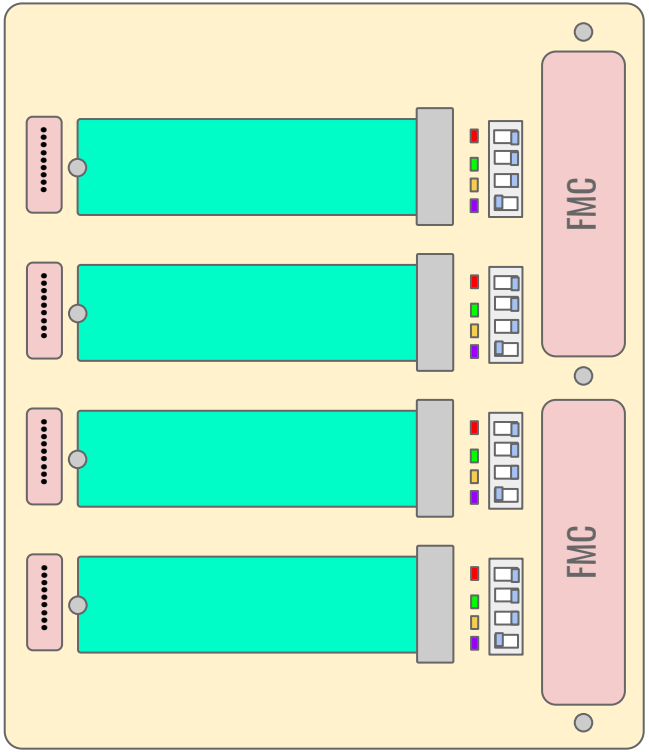
DOKARD`S SERVICE SIGNALS

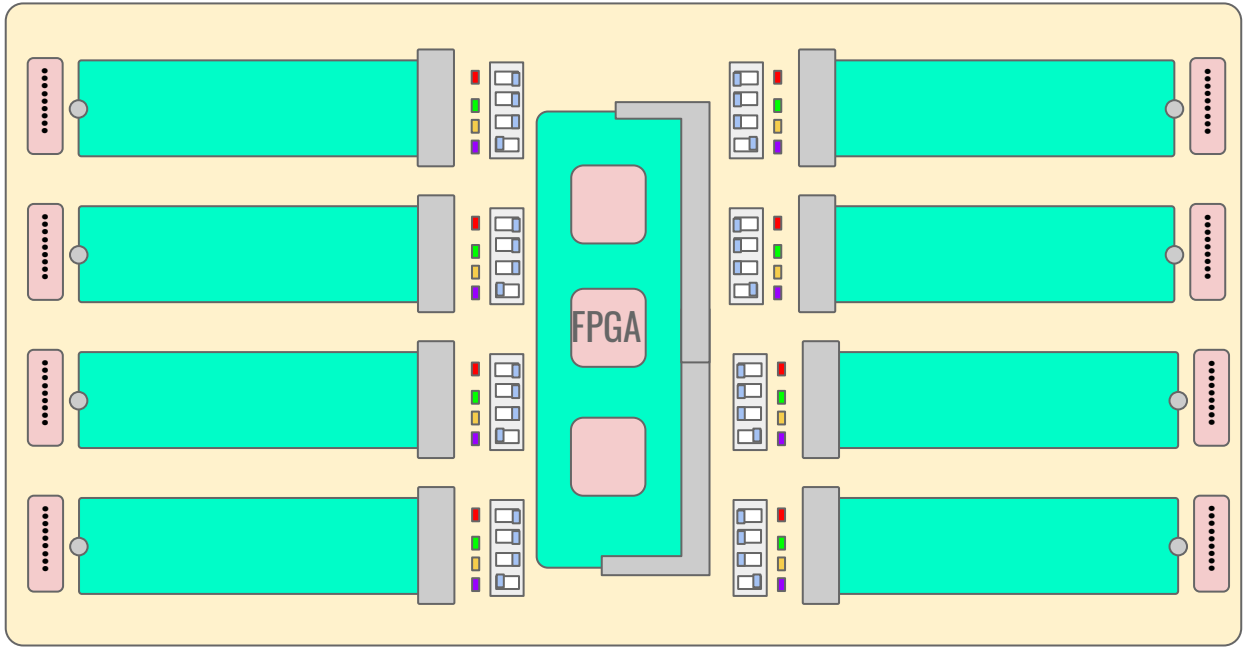
1. MA[0:2] - Module address (to I2C EEPROM or/and future use)
2. I2C - Plug & Play config from I2C EEPROM
3. CLK P/N - Clock's differential pair or two single ended clocks
4. Vadj - DC/DC to produce required voltage level (same as FMC)
5. PWR_EN/RESET - Power enable for module and reset (both are redundant)
6. LED[0:3] - For indications onto mainboard
7. DIP[0:3] - To set up settings from mainboard's DIP switches
8. TERMINAL[0:7] - Mainboard's EXTernal connector (IDC or most proper should be considering)
9. USB DP/DM - To mainboards USB-hub/USB-connector

ROADMAP

- A kind of several types of boards:
  - Low cost (1-layer PCB solution w/o P&P)
  - “Standard” (LPC & HPC as in FMC)
  - HighSpeed (replica of NVMe-pinout for example)
- Enhancement plug&play capabilities (inspired by Litex and IPMI)
- Design FMC-to-DOKARD PCB adapter
- Design FPGA DevKit with DOKARD mezzanine supports
  - Based on FPGA SoM
  - Allow 2 layer PCB to demonstrate convenience*

ROADMAP



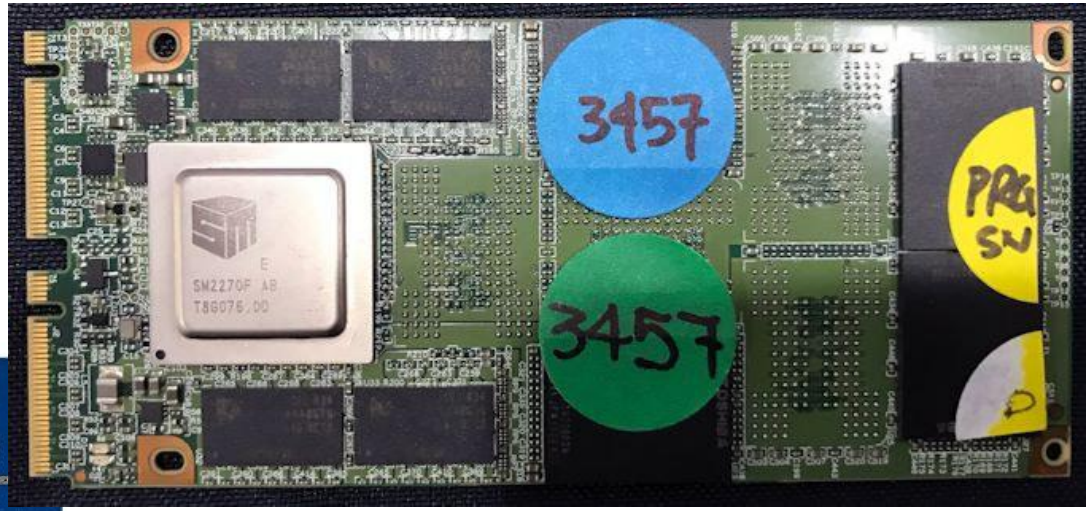


UNDER CONSIDERATION

- Right place and principles of using signal level shifters
- Compatibility issue: should we use NGFF M-key for HighSpeed edition (e.g. for NVMe SSD bolt-on) in addition of NGFF B-key usage
- Scalability: implementing of cards teaming by 1x, 2x, 4x (see next slide)
- Mechanical uncertainty:
  - Card's length dimensions (currently: only 30mm and 80mm)
  - Card's width dimensions (NGFF refs: 22mm and 30mm)
  - Mounting methods
  - On-card connectors placement (hot topic)

UNDER CONSIDERATION

Non-NGFF dimensions and mountings



Cards teaming by 2x (increase the available pins count)

FEEDBACK / REFERENCES*

github.com/dokard

t.me/dokard_chat

CONCLUSION

PROS:

- ❏ Nearly Zero Waste
- ❏ Rapid time-to-deploy
- ❏ Daughter boards as cheap as possible
- ❏ Flexibility in terms of purpose usage
- ❏ Powerful Plug and Play capabilities

CONS:

- ❏ 0.8mm PCB thickness required
- ❏ Highly recommend special finishing for PCB
- ❏ Relatively low mechanical hardness (PCB strength)
- ❏ Poor availability of DOKARD boards (hopefully temporary)

DISCOVER.
DESIGN.
DEVELOP.

yadro.com

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tech@exponenta.ru
exponenta.ru

ЭКСПОНЕНТА

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- Подбор **инструментов**
- **Обучение** специалистов
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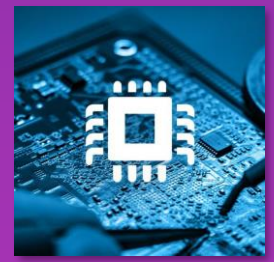

НОВОСТИ МИРА ЭК

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