

III КОНФЕРЕНЦИЯ FPGA РАЗРАБОТЧИКОВ

FPGA-Systems 2021.2

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Поддержи мероприятие

Способ 1

Способ 2



Intel® Agilex™ FPGA Design Seminars

High-Speed Serial Interfaces in Intel® Agilex™ FPGAs

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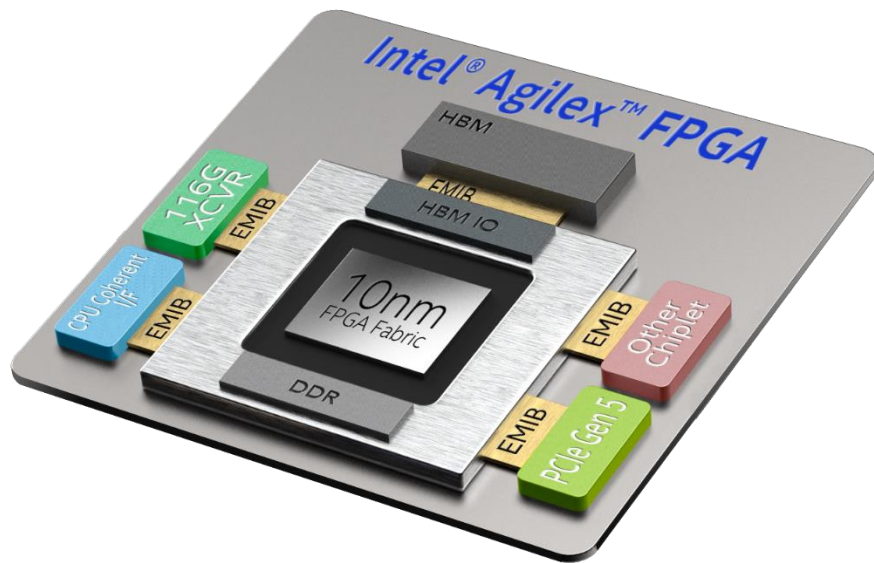
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Agenda

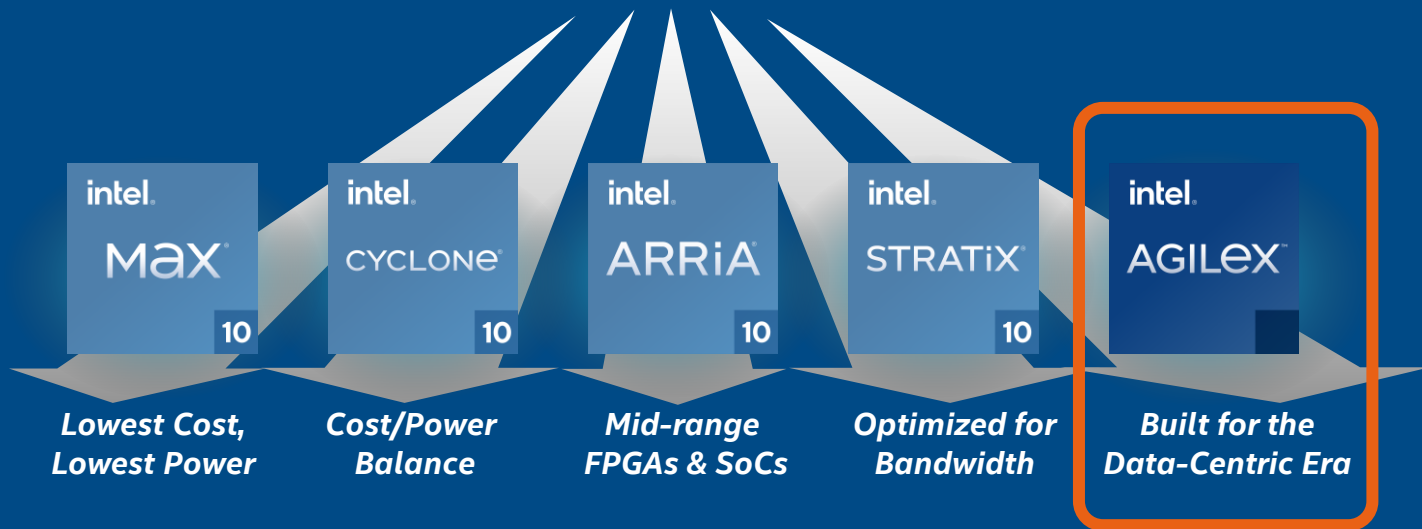
- Intel® Agilex Overview
- Transceiver Tiles
- Transceiver Toolkit & Other Tools
- Q&A



Intel® Agilex® Overview



Intel® FPGA Portfolio



Intel® FPGAs and SoC FPGAs for Every Application

The FPGA for the Data-Centric World

Process Data

2nd
Generation
Intel®
Hyperflex™
Architecture

Up to
40%
Higher^{1,3}
performance

Up to
40%
Lower^{1,3}
Power

Up to
40 TFLOPS
DSP Performance^{2,3}

Store Data

DDR5 SDRAM
& High-Bandwidth
Memory (HBM)
support

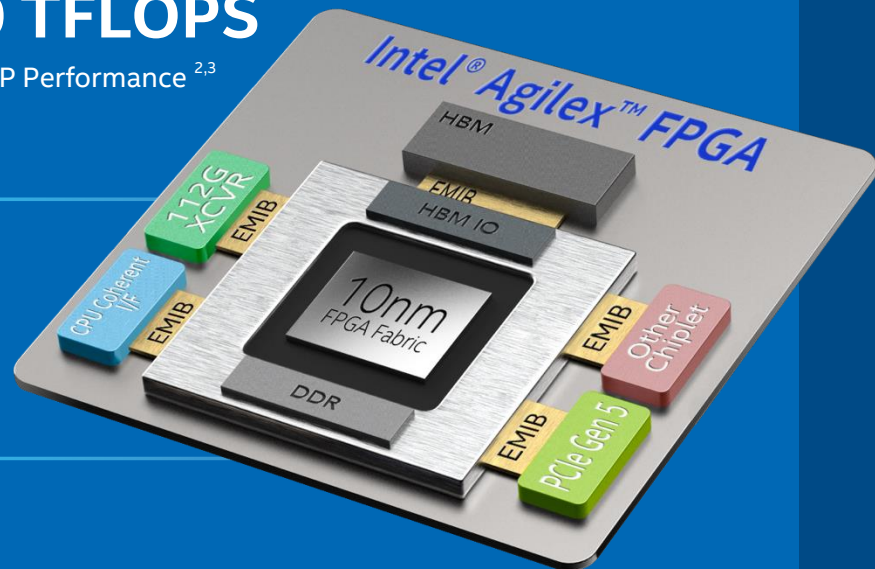
Intel® Optane™
Persistent
Memory support

Move Data



Intel® Xeon® Processor coherent
connectivity & PCIe* Gen5

116G
Transceiver
data rates



¹ Compared to Intel® Stratix® 10 FPGAs

² With FP16 configuration

³ Based on current estimates, see backup for details

The FPGA for the Data-Centric World

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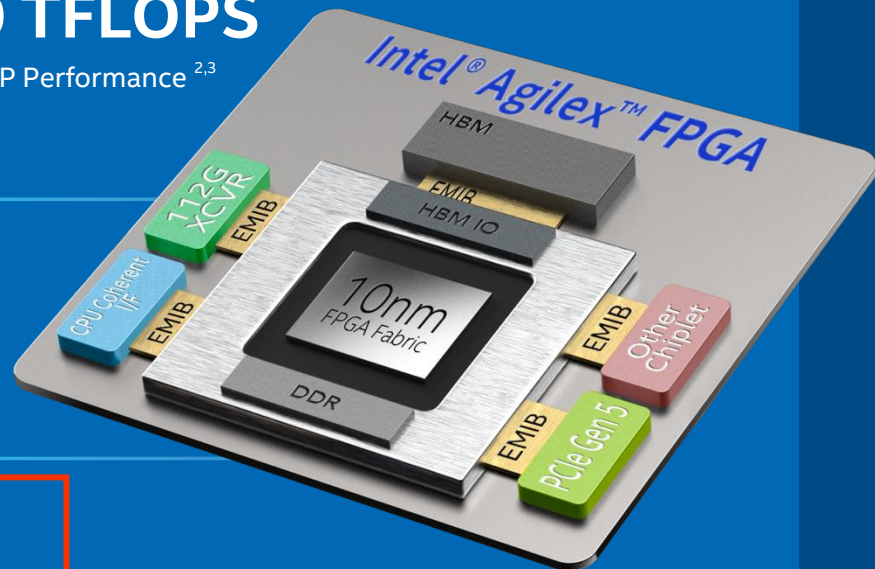
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Intel® EMIB – Enabling Multi-Die Devices

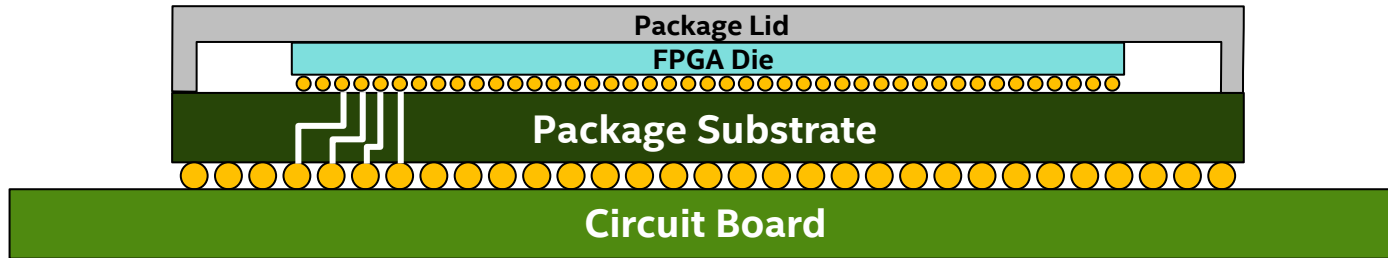


Figure 1. Standard BGA Packaging Technology

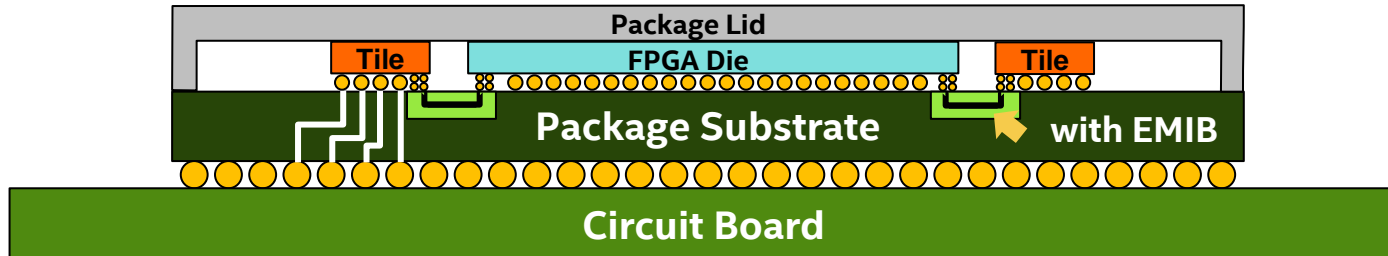
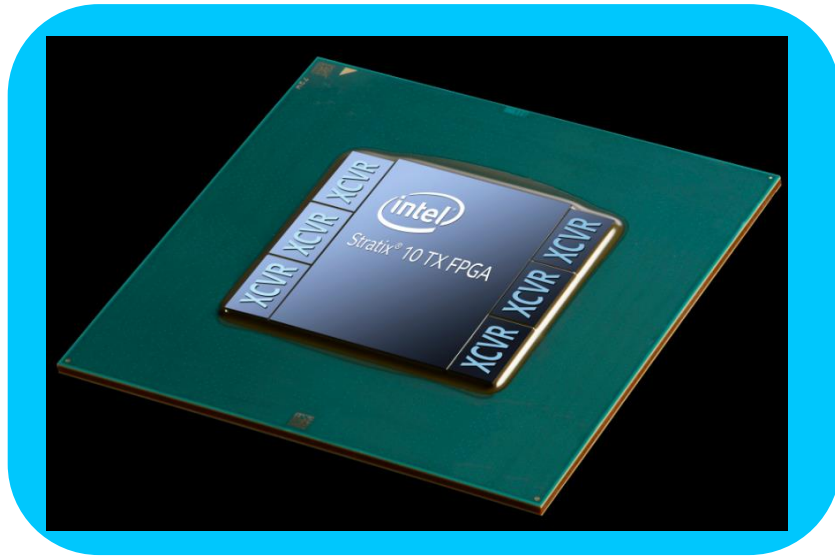
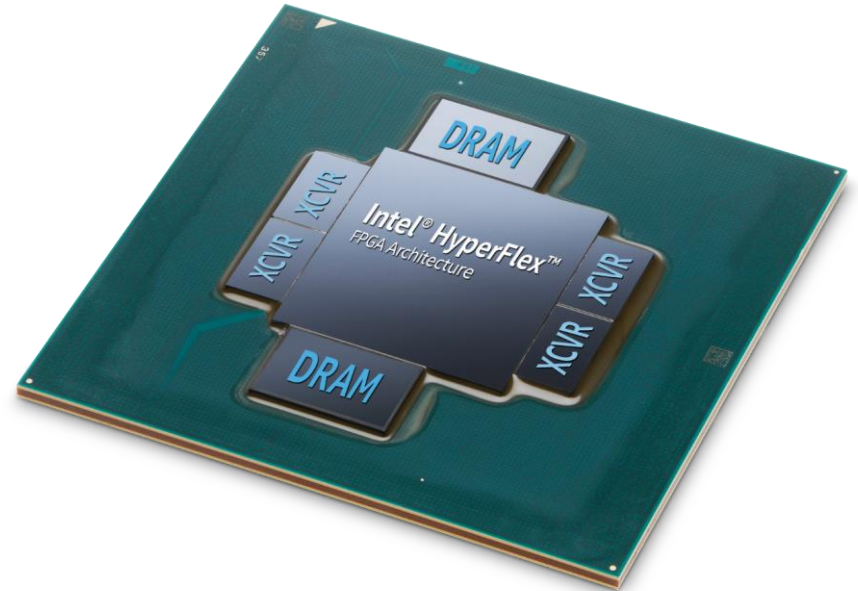


Figure 2. Intel® EMIB (Embedded Multi-Die Interconnect Bridge) Packaging Technology

Intel® Stratix® 10 Devices (Package Lids Removed)



Stratix® 10 TX, E-Tile + H-Tile



Stratix® 10 MX, E-Tile + H-Tile + HBM

Intel® Agilex™ FPGA Family Variants

F - Series

For wide range of applications

Up to 58Gbps Transceivers

PCIe Gen 4

DDR4 Memory Support

Quad Core Arm® Cortex A53
(optional)

I - Series

For high-performance
processor interface and
bandwidth-intensive applications

Coherent attach to Intel®
Xeon® Scalable Processor
(CXL)

Up to 116Gbps Transceivers

PCIe Gen 5

DDR4 Memory Support

Quad Core Arm® Cortex A53

M - Series

For compute-intensive
applications

High bandwidth memory
(HBM) option

Coherent attach to Intel®
Xeon® Scalable Processor
(CXL)

Up to 116Gbps Transceivers

PCIe Gen 5

DDR4, DDR5, Intel®
Optane™ Persistent
Memory support

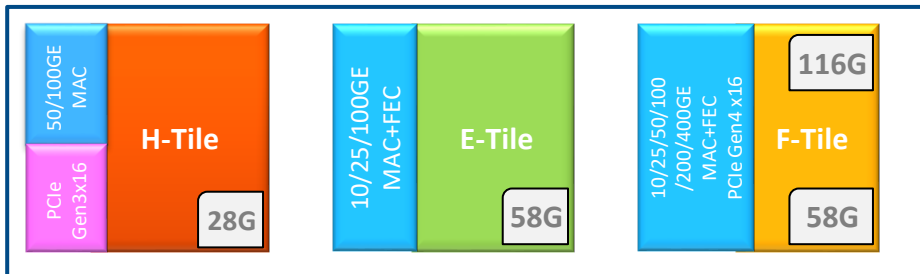
Quad Core Arm® Cortex A53

Transceiver Tiles

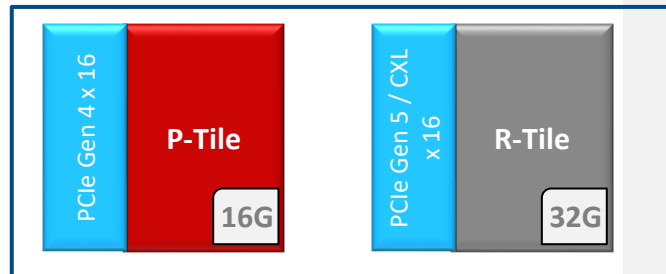


Agilex™ Transceiver Tile Overview

Networking & Communication Tiles



Processor Attach Tiles

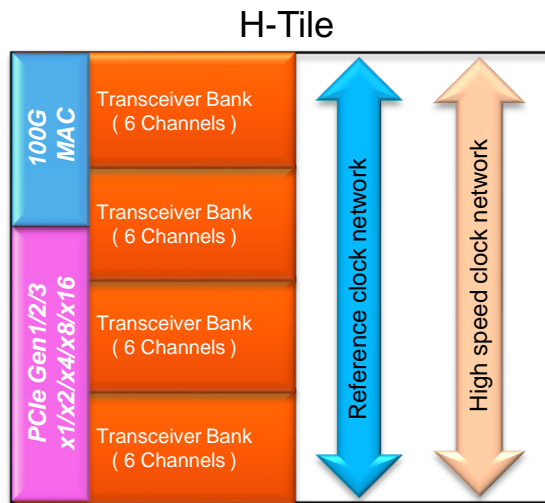


| XCVR Tile Options | H-Tile | E-Tile | F-Tile | P-Tile | R-Tile |
|-------------------------------------|--|---|--|--|---|
| Maximum Data Rate and Channel Count | 16 x 28.3G NRZ or 24 x 17.4G NRZ | 12 x 57.8G PAM4 or 24 x 28.9G NRZ | (FHT) 4 x 116G PAM4 plus (FGT) 12 x 58G PAM4 or 16 x 32G NRZ | 16 x 16G NRZ | 16 x 32G NRZ |
| Hard IP | PCIe* Gen3 x16 with 4 PF/2K VF SR-IOV 50/100GbE MAC and PCS | 10/25/100GbE MAC, PCS and KR/KP RSFEC | PCIe Gen4 x16 EP/RP 8 PF/2K VF SR-IOV 10/25/50/100/200/400GbE MAC, PCS & KR/KP RSFEC | PCIe Gen4 x16 EP/RP 8 PF/2K VF SR-IOV, VirtIO | PCIe Gen5 x16 EP/RP 8 PF/2K VF SR-IOV, SIOV, SVM, VirtIO CXL v1.1 interface PIPE v5.1.1 |
| | In Production (Stratix® 10) | In Production (Stratix® 10) | New for Intel® Agilex™ FPGAs | In Production (Stratix® 10) | New for Intel® Agilex™ FPGAs |

H-Tile Architecture

- H-Tile contains all analog and digital circuits to develop high speed data interfaces
 - 24 transceiver channels
 - PLLs
 - Clock networks
 - Hard IP blocks
 - 1x PCIe Gen3 (w/SR-IOV)
 - 4 Physical Functions, 2K Virtual Functions
 - 1x100G Ethernet
 - 100 GbE MAC

| Feature | H-Tile |
|--------------------|------------------------|
| Total Transceivers | 24 per tile |
| Max Chip-to-Chip | 28.3G NRZ |
| # at Max Rate | 16 @ 28.3G + 8 @ 17.4G |
| Max Backplane | 28.3G up to 30 dB |



E-Tile Architecture

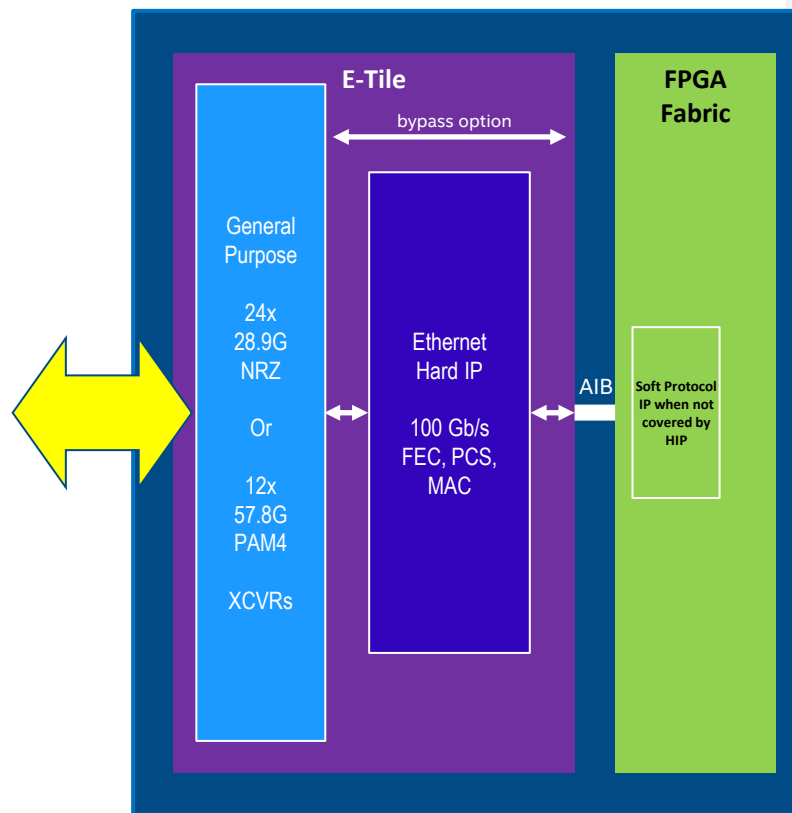
General Purpose

- 24 XCVR channels @ 28.9Gbps NRZ
or
12 XCVR channels @ 57.8Gbps PAM4
- Multi-protocol support for CEI, Ethernet, CPRI, FlexE, Interlaken, Fibre Channel, SRIO, Serial Lite, OTN, JESD204B/C, FlexO

Networking: 100 GbE

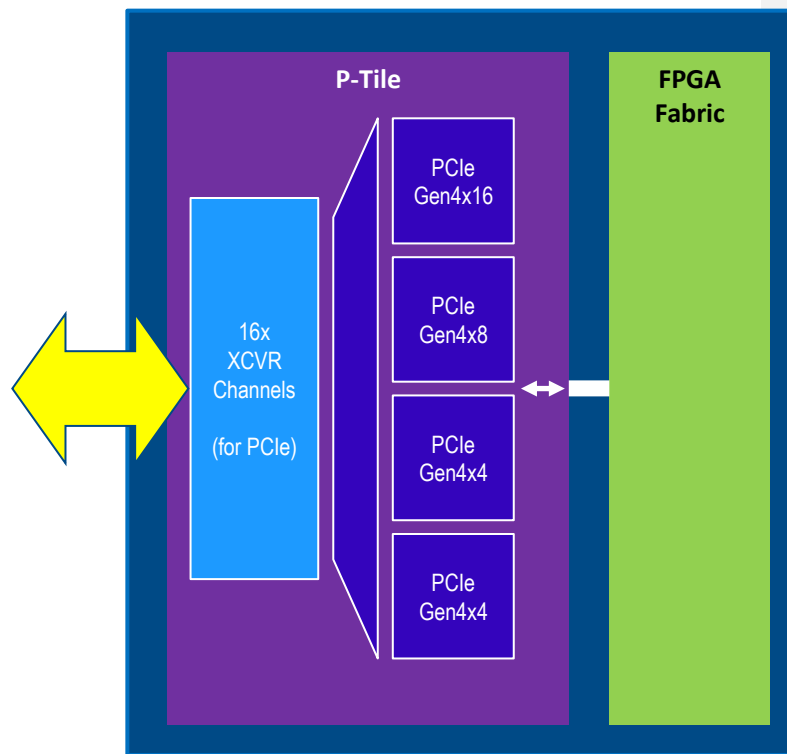
- 24 x 10/25 GbE FEC/PCS/MAC
- 4 x 100 GbE FEC/PCS/MAC
 - 6x RS-FEC
 - 6x KP-FEC⁽¹⁾
- IEEE 1588 support (Precision Time Protocol)

⁽¹⁾ Only 4 instances of KP-FEC are supported when using 100GbE MAC



P-Tile Architecture

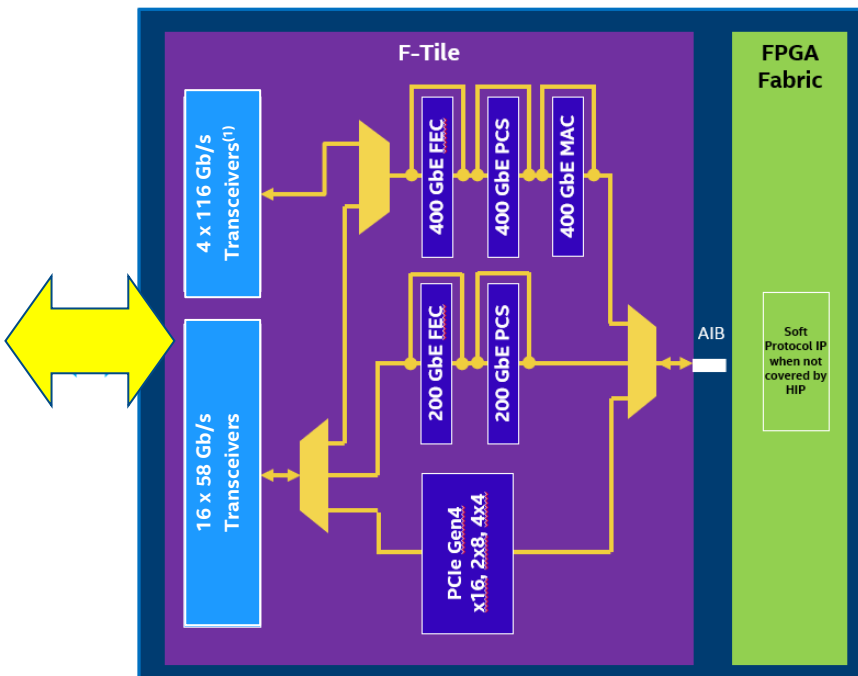
- PCIe Gen4 x16 – 2x bandwidth versus H-Tile
 - PCIe Gen4 x16-lanes up to 16 GT/s (End Point or Root Port)
 - Port Bifurcation support: 2x8 (EP only) or 4x4 (RP only)
 - Optimized for lower latency & higher performance
 - Enhanced Virtualization
 - SR-IOV supporting 8 PFs/2048 VFs
- CvP Initialization, Autonomous HIP
- VirtIO support
- Scalable IOV
- Shared Virtual Memory



Generic protocols and hard IP bypass NOT supported on P-tile

F-Tile Architecture

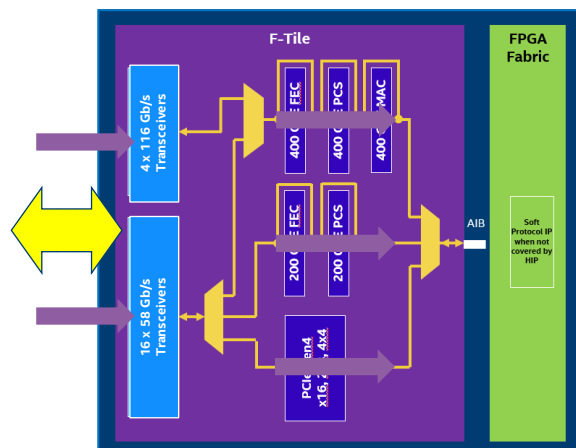
- **XCVR Support**
 - High-Speed XCVRs
 - FHT: 4 channels 96-116Gbps PAM4⁽¹⁾
 - Or 48-58Gbps NRZ/PAM4 or 24-29Gbps NRZ
 - FGT: General Purpose XCVRs
 - 16 channels 1-32Gbps NRZ
 - or 12 channels 20-58Gbps PAM4
 - PMA Direct Mode
- **PCIe Gen4 x16**
 - P-Tile feature set plus:
 - Precise Time Management
- **Advanced Networking Support: 400 GbE**
 - IEEE 1588 support
 - 10/25/50/100/200/400 GbE FEC/PCS/MAC
 - 600G Interlaken
- **General Purpose**
 - Multi-protocol support for CEI, Ethernet, CPRI, JESD204B/C, FlexE, Interlaken, Fibre Channel, InfiniBand, SRIO, Serial Lite, PCIe, GPON, FlexO, SDI, OTN, HDMI, DisplayPort



(1) Not supported in Agilex™ F-series devices

F-Tile Topologies

- F-Tile supports 15 defined system level topologies across:
 - Three separate bifurcatable datapath's, 400G, 200G & PCIe paths
 - Two XCVR blocks, High Speed (FHT), 116Gbps and General Purpose (FGT), 58Gbps sources

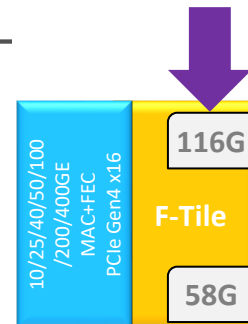


(1) I-Series devices only

| Supported Datapath Configuration | | | | | | |
|----------------------------------|--------------------|---------------|---------------|----------|---------------|-----------------|
| # | 400G DataPath | | 200G DataPath | | PCIe Datapath | |
| | XCVR | Mode | XCVR | Mode | XCVR | Mode |
| 0 | <i>n/a</i> | Disabled | <i>n/a</i> | Disabled | <i>n/a</i> | Disabled |
| 1 | <i>n/a</i> | Disabled | <i>n/a</i> | Disabled | FGT | PCIe Gen4 x16 |
| 2 | <i>n/a</i> | Disabled | <i>n/a</i> | Disabled | FGT | 2x PCIe Gen4 x8 |
| 3 | FHT ⁽¹⁾ | 100G-4 w/PTP | <i>n/a</i> | Disabled | FGT | PCIe Gen4 x16 |
| 4 | <i>n/a</i> | Disabled | <i>n/a</i> | Disabled | FGT | 4x PCIe Gen4 x4 |
| 5 | FHT ⁽¹⁾ | 400G-4 | GP | 200G-8 | <i>n/a</i> | Disabled |
| 6 | FHT ⁽¹⁾ | 400G-4 w/PTP | GP | 150G-6 | <i>n/a</i> | Disabled |
| 7 | FHT ⁽¹⁾ | 400G-4 w/PTP | <i>n/a</i> | Disabled | FGT | PCIe Gen4 x4 |
| 8 | FHT ⁽¹⁾ | 250G-4 w/PTP | <i>n/a</i> | Disabled | FGT | PCIe Gen4 x8 |
| 9 | FHT ⁽¹⁾ | 250G-4 w/PTP | <i>n/a</i> | Disabled | FGT | 2x PCIe Gen4 x4 |
| 10 | FGT | 400G-8 | GP | 200G-8 | <i>n/a</i> | Disabled |
| 11 | FGT | 400G-8 w/PTP | GP | 150G-6 | <i>n/a</i> | Disabled |
| 12 | FGT | 275G-8 w/PTP | <i>n/a</i> | Disabled | FGT | PCIe Gen4 x8 |
| 13 | FGT | 275G-8 w/PTP | <i>n/a</i> | Disabled | FGT | 2x PCIe Gen4 x4 |
| 14 | FGT | 400G-12 w/PTP | <i>n/a</i> | Disabled | FGT | PCIe Gen4 x4 |
| 15 | FGT | 400G-16 w/PTP | <i>n/a</i> | Disabled | <i>n/a</i> | Disabled |

Supported Standards and Protocols – FHT

- All 4 High-Speed Transceivers (FHT) independent of each other
- Support Ethernet and CEI standards
- Feeds into 400G Hard IP block for Ethernet & CEI



Supported Standards & Protocols

CEI: 112G PAM4-LR/MR/SR, 56G NRZ/PAM4-XSR, 56G NRZ-USR, 56G PAM4-LR/MR/SR/VSR, 25G-LR, 28G MR/VSR

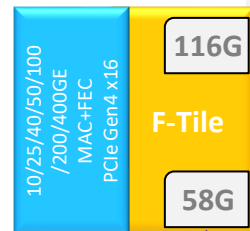
Ethernet (IEEE802.3): 25GbE/50GbE/200GbE/400GbE

SerialLite IV, Interlaken, FlexE, OTN

CEI – Common Electrical I/O

Supported Standards and Protocols – FGT

- All 16 General-Purpose Transceivers independent of each other
- Support many standards and protocols
- Feeds into 200G and 400G Hard IP block, and PCIe block
- Does NOT feed 400G Hard IP block with High-Speed SERDES simultaneously



Supported Standards & Protocols

CEI: 56G PAM4-LR/MR/SR/VSR, 25G-LR, 28G MR/VSR, 11G LR/MR/SR/VSR; 6G LR/SR

Ethernet (IEEE802.3): 10GbE/25GbE/40GbE/50GbE/100GbE/200GbE/400GbE

PCIe Gen1/Gen2/Gen3/Gen4

CPRI, SFF 8431/8418/8402, OTL, OTU, OTN

JESD204B/C, SerialLite IV, FlexE, FlexO

DisplayPort, HDMI, SDI

Interlaken, GPON/EPON, FibreChannel,

SAS, SATA, USB 3.1, V-by-One

F-Tile Documentation



F-tile Architecture and PMA and FEC Direct PHY IP User Guide

Updated for Intel® Quartus® Prime Design Suite: 21.3
IP Version: 3.0.0

06-20215 | 2021.10.15
Send Feedback

1. F-Tile Overview

This user guide describes architecture and implementation details for the Intel® Agilex® F-tile building blocks, physical (PHY) layer IP, PLLs, and clock networks. F-tile has up to 20 PMA per tile, each with integrated advanced high-speed analog signal conditioning and clock data recovery circuits for chip-to-chip, chip-to-module, and backplane applications.

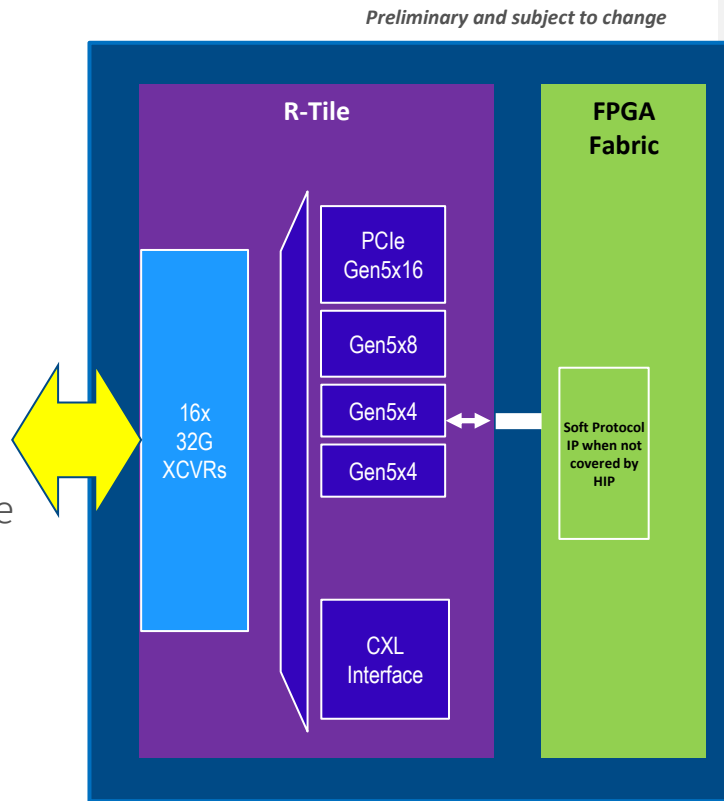
F-tile is a PMA and NRZ dual-mode serial interface tile that contains 16 FGT PMAs and four FHT PMAs. F-tile contains multiple hard IP blocks for use in conjunction with the PMAs to allow efficient implementation of popular and emerging serial protocols. F-tile connects to the FPGA fabric using the Intel embedded multi-die interconnect bridge (EMIB) technology.

Table 1. F-Tile Features

| Feature | Description |
|--|---|
| Number of available PMAs | Up to 20. • FHT: up to four per tile. • FGT: up to 16 per tile. Not all FHT PMAs bond out in every die. Refer to Intel Agilex Device Family Pin Connection Guidelines. |
| Data rate range | PMAs: • 24-28 Gbps NRZ • 40-58 Gbps NRZ and PAM4 • 96-110 Gbps PAM4 FHT: • 1-13 Gbps NRZ • 20-58.125 PAM4 Not all FGT PMAs support the same data rates. Refer to PMA Data Rates. |
| Number of EMIBs | 24 |
| PCIE Hard IP modes | Up to one Gen4 x16, two Gen4 x8, or four Gen4 x4. |
| Ethernet Hard IP modes with number of supported PMAs for each, where (200G6) is 100G mode supporting one PMA | 100G6-1, 200G6-1, 400G6-1, 800G6-1, 100G6-2, 200G6-2, 400G6-2, 800G6-2, 100G6-3, 200G6-3, 400G6-3, 800G6-3, 100G6-4, 200G6-4, 400G6-4, 800G6-4, 100G6-5, 200G6-5, 400G6-5, 800G6-5, 100G6-6, 200G6-6, 400G6-6, 800G6-6, 100G6-7, 200G6-7, 400G6-7, 800G6-7, 100G6-8, 200G6-8, 400G6-8, 800G6-8, 100G6-9, 200G6-9, 400G6-9, 800G6-9, 100G6-10, 200G6-10, 400G6-10, 800G6-10, 100G6-11, 200G6-11, 400G6-11, 800G6-11, 100G6-12, 200G6-12, 400G6-12, 800G6-12, 100G6-13, 200G6-13, 400G6-13, 800G6-13, 100G6-14, 200G6-14, 400G6-14, 800G6-14, 100G6-15, 200G6-15, 400G6-15, 800G6-15, 100G6-16, 200G6-16, 400G6-16, 800G6-16, 100G6-17, 200G6-17, 400G6-17, 800G6-17, 100G6-18, 200G6-18, 400G6-18, 800G6-18, 100G6-19, 200G6-19, 400G6-19, 800G6-19, 100G6-20, 200G6-20, 400G6-20, 800G6-20, 100G6-21, 200G6-21, 400G6-21, 800G6-21, 100G6-22, 200G6-22, 400G6-22, 800G6-22, 100G6-23, 200G6-23, 400G6-23, 800G6-23, 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100G6-74, 200G6-74, 400G6-74, 800G6-74, 100G6-75, 200G6-75, 400G6-75, 800G6-75, 100G6-76, 200G6-76, 400G6-76, 800G6-76, 100G6-77, 200G6-77, 400G6-77, 800G6-77, 100G6-78, 200G6-78, 400G6-78, 800G6-78, 100G6-79, 200G6-79, 400G6-79, 800G6-79, 100G6-80, 200G6-80, 400G6-80, 800G6-80, 100G6-81, 200G6-81, 400G6-81, 800G6-81, 100G6-82, 200G6-82, 400G6-82, 800G6-82, 100G6-83, 200G6-83, 400G6-83, 800G6-83, 100G6-84, 200G6-84, 400G6-84, 800G6-84, 100G6-85, 200G6-85, 400G6-85, 800G6-85, 100G6-86, 200G6-86, 400G6-86, 800G6-86, 100G6-87, 200G6-87, 400G6-87, 800G6-87, 100G6-88, 200G6-88, 400G6-88, 800G6-88, 100G6-89, 200G6-89, 400G6-89, 800G6-89, 100G6-90, 200G6-90, 400G6-90, 800G6-90, 100G6-91, 200G6-91, 400G6-91, 800G6-91, 100G6-92, 200G6-92, 400G6-92, 800G6-92, 100G6-93, 200G6-93, 400G6-93, 800G6-93, 100G6-94, 200G6-94, 400G6-94, 800G6-94, 100G6-95, 200G6-95, 400G6-95, 800G6-95, 100G6-96, 200G6-96, 400G6-96, 800G6-96, 100G6-97, 200G6-97, 400G6-97, 800G6-97, 100G6-98, 200G6-98, 400G6-98, 800G6-98, 100G6-99, 200G6-99, 400G6-99, 800G6-99, 100G6-100, 200G6-100, 400G6-100, 800G6-100, 100G6-101, 200G6-101, 400G6-101, 800G6-101, 100G6-102, 200G6-102, 400G6-102, 800G6-102, 100G6-103, 200G6-103, 400G6-103, 800G6-103, 100G6-104, 200G6-104, 400G6-104, 800G6-104, 100G6-105, 200G6-105, 400G6-105, 800G6-105, 100G6-106, 200G6-106, 400G6-106, 800G6-106, 100G6-107, 200G6-107, 400G6-107, 800G6-107, 100G6-108, 200G6-108, 400G6-108, 800G6-108, 100G6-109, 200G6-109, 400G6-109, 800G6-109, 100G6-110, 200G6-110, 400G6-110, 800G6-110, 100G6-111, 200G6-111, 400G6-111, 800G6-111, 100G6-112, 200G6-112, 400G6-112, 800G6-112, 100G6-113, 200G6-113, 400G6-113, 800G6-113, 100G6-114, 200G6-114, 400G6-114, 800G6-114, 100G6-115, 200G6-115, 400G6-115, 800G6-115, 100G6-116, 200G6-116, 400G6-116, 800G6-116, 100G6-117, 200G6-117, 400G6-117, 800G6-117, 100G6-118, 200G6-118, 400G6-118, 800G6-118, 100G6-119, 200G6-119, 400G6-119, 800G6-119, 100G6-120, 200G6-120, 400G6-120, 800G6-120, 100G6-121, 200G6-121, 400G6-121, 800G6-121, 100G6-122, 200G6-122, 400G6-122, 800G6-122, 100G6-123, 200G6-123, 400G6-123, 800G6-123, 100G6-124, 200G6-124, 400G6-124, 800G6-124, 100G6-125, 200G6-125, 400G6-125, 800G6-125, 100G6-126, 200G6-126, 400G6-126, 800G6-126, 100G6-127, 200G6-127, 400G6-127, 800G6-127, 100G6-128, 200G6-128, 400G6-128, 800G6-128, 100G6-129, 200G6-129, 400G6-129, 800G6-129, 100G6-130, 200G6-130, 400G6-130, 800G6-130, 100G6-131, 200G6-131, 400G6-131, 800G6-131, 100G6-132, 200G6-132, 400G6-132, 800G6-132, 100G6-133, 200G6-133, 400G6-133, 800G6-133, 100G6-134, 200G6-134, 400G6-134, 800G6-134, 100G6-135, 200G6-135, 400G6-135, 800G6-135, 100G6-136, 200G6-136, 400G6-136, 800G6-136, 100G6-137, 200G6-137, 400G6-137, 800G6-137, 100G6-138, 200G6-138, 400G6-138, 800G6-138, 100G6-139, 200G6-139, 400G6-139, 800G6-139, 100G6-140, 200G6-140, 400G6-140, 800G6-140, 100G6-141, 200G6-141, 400G6-141, 800G6-141, 100G6-142, 200G6-142, 400G6-142, 800G6-142, 100G6-143, 200G6-143, 400G6-143, 800G6-143, 100G6-144, 200G6-144, 400G6-144, 800G6-144, 100G6-145, 200G6-145, 400G6-145, 800G6-145, 100G6-146, 200G6-146, 400G6-146, 800G6-146, 100G6-147, 200G6-147, 400G6-147, 800G6-147, 100G6-148, 200G6-148, 400G6-148, 800G6-148, 100G6-149, 200G6-149, 400G6-149, 800G6-149, 100G6-150, 200G6-150, 400G6-150, 800G6-150, 100G6-151, 200G6-151, 400G6-151, 800G6-151, 100G6-152, 200G6-152, 400G6-152, 800G6-152, 100G6-153, 200G6-153, 400G6-153, 800G6-153, 100G6-154, 200G6-154, 400G6-154, 800G6-154, 100G6-155, 200G6-155, 400G6-155, 800G6-155, 100G6-156, 200G6-156, 400G6-156, 800G6-156, 100G6-157, 200G6-157, 400G6-157, 800G6-157, 100G6-158, 200G6-158, 400G6-158, 800G6-158, 100G6-159, 200G6-159, 400G6-159, 800G6-159, 100G6-160, 200G6-160, 400G6-160, 800G6-160, 100G6-161, 200G6-161, 400G6-161, 800G6-161, 100G6-162, 200G6-162, 400G6-162, 800G6-162, 100G6-163, 200G6-163, 400G6-163, 800G6-163, 100G6-164, 200G6-164, 400G6-164, 800G6-164, 100G6-165, 200G6-165, 400G6-165, 800G6-165, 100G6-166, 200G6-166, 400G6-166, 800G6-166, 100G6-167, 200G6-167, 400G6-167, 800G6-167, 100G6-168, 200G6-168, 400G6-168, 800G6-168, 100G6-169, 200G6-169, 400G6-169, 800G6-169, 100G6-170, 200G6-170, 400G6-170, 800G6-170, 100G6-171, 200G6-171, 400G6-171, 800G6-171, 100G6-172, 200G6-172, 400G6-172, 800G6-172, 100G6-173, 200G6-173, 400G6-173, 800G6-173, 100G6-174, 200G6-174, 400G6-174, 800G6-174, 100G6-175, 200G6-175, 400G6-175, 800G6-175, 100G6-176, 200G6-176, 400G6-176, 800G6-176, 100G6-177, 200G6-177, 400G6-177, 800G6-177, 100G6-178, 200G6-178, 400G6-178, 800G6-178, 100G6-179, 200G6-179, 400G6-179, 800G6-179, 100G6-180, 200G6-180, 400G6-180, 800G6-180, 100G6-181, 200G6-181, 400G6-181, 800G6-181, 100G6-182, 200G6-182, 400G6-182, 800G6-182, 100G6-183, 200G6-183, 400G6-183, 800G6-183, 100G6-184, 200G6-184, 400G6-184, 800G6-184, 100G6-185, 200G6-185, 400G6-185, 800G6-185, 100G6-186, 200G6-186, 400G6-186, 800G6-186, 100G6-187, 200G6-187, 400G6-187, 800G6-187, 100G6-188, 200G6-188, 400G6-188, 800G6-188, 100G6-189, 200G6-189, 400G6-189, 800G6-189, 100G6-190, 200G6-190, 400G6-190, 800G6-190, 100G6-191, 200G6-191, 400G6-191, 800G6-191, 100G6-192, 200G6-192, 400G6-192, 800G6-192, 100G6-193, 200G6-193, 400G6-193, 800G6-193, 100G6-194, 200G6-194, 400G6-194, 800G6-194, 100G6-195, 200G6-195, 400G6-195, 800G6-195, 100G6-196, 200G6-196, 400G6-196, 800G6-196, 100G6-197, 200G6-197, 400G6-197, 800G6-197, 100G6-198, 200G6-198, 400G6-198, 800G6-198, 100G6-199, 200G6-199, 400G6-199, 800G6-199, 100G6-200, 200G6-200, 400G6-200, 800G6-200, 100G6-201, 200G6-201, 400G6-201, 800G6-201, 100G6-202, 200G6-202, 400G6-202, 800G6-202, 100G6-203, 200G6-203, 400G6-203, 800G6-203, 100G6-204, 200G6-204, 400G6-204, 800G6-204, 100G6-205, 200G6-205, 400G6-205, 800G6-205, 100G6-206, 200G6-206, 400G6-206, 800G6-206, 100G6-207, 200G6-207, 400G6-207, 800G6-207, 100G6-208, 200G6-208, 400G6-208, 800G6-208, 100G6-209, 200G6-209, 400G6-209, 800G6-209, 100G6-210, 200G6-210, 400G6-210, 800G6-210, 100G6-211, 200G6-211, 400G6-211, 800G6-211, 100G6-212, 200G6-212, 400G6-212, 800G6-212, 100G6-213, 200G6-213, 400G6-213, 800G6-213, 100G6-214, 200G6-214, 400G6-214, 800G6-214, 100G6-215, 200G6-215, 400G6-215, 800G6-215, 100G6-216, 200G6-216, 400G6-216, 800G6-216, 100G6-217, 200G6-217, 400G6-217, 800G6-217, 100G6-218, 200G6-218, 400G6-218, 800G6-218, 100G6-219, 200G6-219, 400G6-219, 800G6-219, 100G6-220, 200G6-220, 400G6-220, 800G6-220, 100G6-221, 200G6-221, 400G6-221, 800G6-221, 100G6-222, 200G6-222, 400G6-222, 800G6-222, 100G6-223, 200G6-223, 400G6-223, 800G6-223, 100G6-224, 200G6-224, 400G6-224, 800G6-224, 100G6-225, 200G6-225, 400G6-225, 800G6-225, 100G6-226, 200G6-226, 400G6-226, 800G6-226, 100G6-227, 200G6-227, 400G6-227, 800G6-227, 100G6-228, 200G6-228, 400G6-228, 800G6-228, 100G6-229, 200G6-229, 400G6-229, 800G6-229, 100G6-230, 200G6-230, 400G6-230, 800G6-230, 100G6-231, 200G6-231, 400G6-231, 800G6-231, 100G6-232, 200G6-232, 400G6-232, 800G6-232, 100G6-233, 200G6-233, 400G6-233, 800G6-233, 100G6-234, 200G6-234, 400G6-234, 800G6-234, 100G6-235, 200G6-235, 400G6-235, 800G6-235, 100G6-236, 200G6-236, 400G6-236, 800G6-236, 100G6-237, 200G6-237, 400G6-237, 800G6-237, 100G6-238, 200G6-238, 400G6-238, 800G6-238, 100G6-239, 200G6-239, 400G6-239, 800G6-239, 100G6-240, 200G6-240, 400G6-240, 800G6-240, 100G6-241, 200G6-241, 400G6-241, 800G6-241, 100G6-242, 200G6-242, 400G6-242, 800G6-242, 100G6-243, 200G6-243, 400G6-243, 800G6-243, 100G6-244, 200G6-244, 400G6-244, 800G6-244, 100G6-245, 200G6-245, 400G6-245, 800G6-245, 100G6-246, 200G6-246, 400G6-246, 800G6-246, 100G6-247, 200G6-247, 400G6-247, 800G6-247, 100G6-248, 200G6-248, 400G6-248, 800G6-248, 100G6-249, 200G6-249, 400G6-249, 800G6-249, 100G6-250, 200G6-250, 400G6-250, 800G6-250, 100G6-251, 200G6-251, 400G6-251, 800G6-251, 100G6-252, 200G6-252, 400G6-252, 800G6-252, 100G6-253, 200G6-253, 400G6-253, 800G6-253, 100G6-254, 200G6-254, 400G6-254, 800G6-254, 100G6-255, 200G6-255, 400G6-255, 800G6-255, 100G6-256, 200G6-256, 400G6-256, 800G6-256, 100G6-257, 200G6-257, 400G6-257, 800G6-257, 100G6-258, 200G6-258, 400G6-258, 800G6-258, 100G6-259, 200G6-259, 400G6-259, 800G6-259, 100G6-260, 200G6-260, 400G6-260, 800G6-260, 100G6-261, 200G6-261, 400G6-261, 800G6-261, 100G6-262, 200G6-262, 400G6-262, 800G6-262, 100G6-263, 200G6-263, 400G6-263, 800G6-263, 100G6-264, 200G6-264, 400G6-264, 800G6-264, 100G6-265, 200G6-265, 400G6-265, 800G6-265, 100G6-266, 200G6-266, 400G6-266, 800G6-266, 100G6-267, 200G6-267, 400G6-267, 800G6-267, 100G6-268, 200G6-268, 400G6-268, 800G6-268, 100G6-269, 200G6-269, 400G6-269, 800G6-269, 100G6-270, 200G6-270, 400G6-270, 800G6-270, 100G6-271, 200G6-271, 400G6-271, 800G |

R-Tile Architecture

- Compute Express Link (CXL)
 - Low latency, coherency for high-performance acceleration
- PCIe Gen5 x16-lanes up to 32G (EP or RP)
 - Port Bifurcation support: 2x8 EP or 4x4 RP
- CvP Initialization, Autonomous HIP
- Separate header and payload interfaces on user interface
- Virtualization (SR-IOV) supporting 8 PFs/2k VFs
- Scalable IOV
- Shared virtual memory
- VirtIO Support
- Precise Time Management
- PMA PIPE



R-Tile can be configured to operate in either PCIe **OR** CXL mode, but not both simultaneously

Transceiver Toolkit & Other Tools



Transceiver Toolkit Overview

The Transceiver Toolkit (TTK) is a powerful analog verification tool

- Quickly analyzes the transceiver signal quality and performance
- Generates and checks pseudo-random binary sequence (PRBS) patterns to measure the BER
- Dynamically changes transceiver buffer settings under automatic or manual control
- Creates eye diagrams at RX for NRZ and PAM4 modulation
- Supports a variety of design situations
- Comes free with any licensed version of the Intel® Quartus® Prime software

Transceiver Toolkit GUI

System Console <@pg-iccf0265>

Transceiver Link: LINK[2]slave_10000[S10_4chan_25g_6chl_4D][S10_native_phy_6chl]0

Toolkit Explorer | **System Explorer**

Instances: /data/kkwong/stratix10/toolkit/t...
 top.sof
 USB-BlasterII on pg-malabpc29 [USB-1]
 1SG280LU2F50I2LG
 S10_4chan_25g_6chl_4D
 S10_native_phy_3chl
 S10_native_phy_6chl

References: /data/kkwong/stratix10/toolkit/t...
 ltile_htile_nphy_toolkit_1.0
 ltile_htile_nphy_toolkit_1.0

Details | **Collections**

L/H-Tile Native Phy Toolkit
 RX Channel 0
 RX Channel 1
 RX Channel 2
 TX Channel 0
 TX Channel 1
 TX Channel 2

collection_1
 L/H-Tile Native Phy Toolkit
 USB-BlasterII on pg-malabpc29 [U...]
 RX Channel 0
 RX Channel 1
 RX Channel 2
 TX Channel 0
 TX Channel 1
 TX Channel 2

collection_2
 L/H-Tile Native Phy Toolkit
 USB-BlasterII on pg-malabpc29 [U...]
 RX Channel 0
 RX Channel 1
 RX Channel 2
 TX Channel 0
 TX Channel 1
 TX Channel 2

Open Toolkit

Table:

| Instance | Channel | Loopback M... | PRBS pattern | Bit error rat... | Number of b... | VGA DC Gain | CTLE EQ Gain | CTLE AC Gain | DFE | Vod | Pre-emphasi... | Pre-emphasi... |
|--|--------------|-----------------|--------------|------------------|----------------|-------------|--------------|--------------|-----|-----|----------------|----------------|
| <input type="checkbox"/> S10_native_p... | RX Channel 0 | Serial Loopb... | PRBS15 | 0.0 | 0 | 0 | 0 | 0 | Off | N/A | N/A | N/A |
| <input type="checkbox"/> S10_native_p... | RX Channel 1 | Serial Loopb... | PRBS15 | 0.0 | 0 | 0 | 0 | 0 | Off | N/A | N/A | N/A |
| <input type="checkbox"/> S10_native_p... | RX Channel 2 | Serial Loopb... | PRBS15 | 0.0 | 0 | 0 | 0 | 0 | Off | N/A | N/A | N/A |
| <input type="checkbox"/> S10_native_p... | TX Channel 0 | N/A | PRBS15 | N/A | N/A | N/A | N/A | N/A | N/A | 31 | 10 | 0 |
| <input type="checkbox"/> S10_native_p... | TX Channel 1 | N/A | PRBS15 | N/A | N/A | N/A | N/A | N/A | N/A | 31 | 0 | 0 |
| <input type="checkbox"/> S10_native_p... | TX Channel 2 | N/A | PRBS15 | N/A | N/A | N/A | N/A | N/A | N/A | 31 | 0 | 0 |

Toolkit Parameters | **Channel Parameters**

S10_native_phy_3chl

Toolkit: L/H-Tile Native Phy Toolkit (ltile_htile_nphy_toolkit_1.0)
IPs: USB-BlasterII on pg-malabpc29 [USB-1][1SG280HH[152][252][352]...@2][S10_4chan_25g_6chl_4D][S10_native_phy_3chl]kcvr_native_s10_htile_0

L/H-Tile Native Phy Parameterizations

Device OPN: 1SG280LU2F50I2LG
 Device Revision: 14nm5br2b
 Number of Channels soft register: 3
 Duplex Mode soft register: DUPLEX
 Channel Type: GX
 Background Calibration Enabled: 0
 PMA Mode: basic
 Protocol Mode: basic_std

L/H-Tile Native Phy Controls

Reset All Channels
 Refresh All Channels
 Live update refresh period (ms): 1000

Autosweep Settings

Autosweep Case Length (ms): 2000

Identify device OPN, IP instance name and channels, PMA and protocol modes

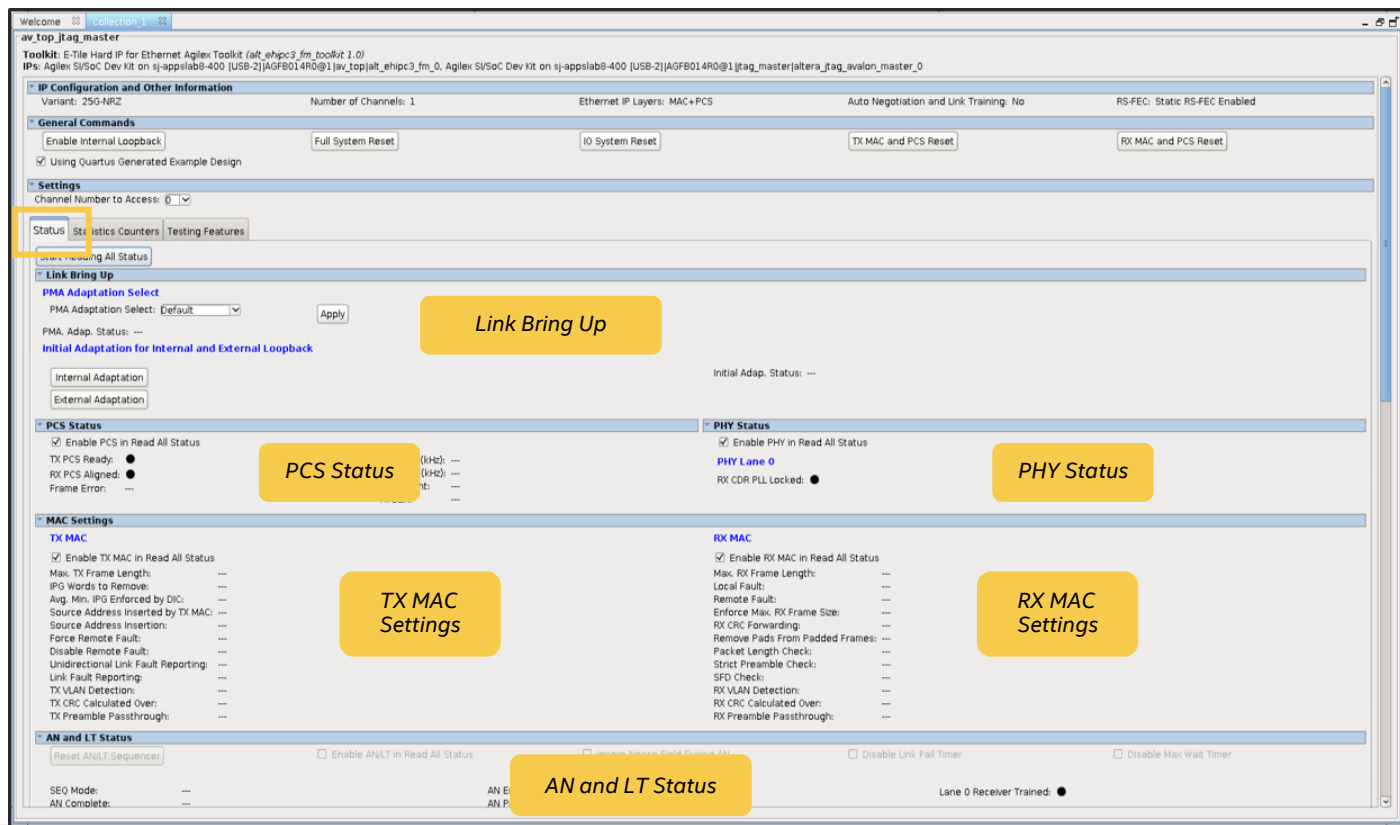
Multiple instances of toolkit can be activated

Ethernet Toolkit

- The Ethernet Toolkit is Intel® FPGA on-chip debugging tool for analyzing real-time status of Ethernet Intel FPGA IP
- Runs on [System Console](#) platform
- Interfaces with Ethernet IP through FPGA's [JTAG connection](#)
- [Continuously monitors IP](#) functions through its registers
- Provides [graphical interface](#) for accessing Ethernet IP and link information

* For more details on using the System Console, see the online training entitled [System Console](#)

Ethernet Toolkit: Status Tab



Ethernet Toolkit: Statistics Counters Tab

The screenshot shows the 'Statistics Counters' tab in the Ethernet Toolkit. The interface is divided into several sections:

- IP Configuration and Other Information:** Shows variant (25G-NR2), number of channels (1), Ethernet IP layers (MAC+PCS), auto negotiation and link training (No), and RS-FEC (Static RS-FEC Enabled).
- General Commands:** Includes buttons for 'Enable Internal Loopback', 'Full System Reset', 'IO System Reset', 'TX MAC and PCS Reset', and 'RX MAC and PCS Reset'.
- Settings:** Includes a 'Channel Number to Access' dropdown (set to 0) and a 'Status' dropdown (set to 'Statistics Counters').
- Example Design Packet Generator Settings:** Includes a 'Packet Generator Modes' section with 'Enable Total Number of Packets' checked, 'Packet Generator Mode' set to 'Random Mode - Random Gap', 'Packet Byte Size - Begin' and 'End' set to 0, and 'Total Number of Packets' set to 0. A yellow callout box labeled 'Example Design Packet Generator Settings' points to this section.
- Source and Destination Addresses:** Includes fields for 'New Source Address', 'Source Address' (0x876543210ADD), 'New Destination Address', and 'Destination Address' (0x123456780ADD). A yellow callout box labeled 'RS-FEC Status and Control' points to the 'Dynamic RS-FEC' section.
- Transmitter and Receiver Statistics:** Includes a table of statistics counters for both TX and RX. A yellow callout box labeled 'TX and RX Statistics' points to this table.
- RS-FEC:** Includes a 'Dynamic RS-FEC' section with a 'Disable RS-FEC' button, an 'Error Injection' section with a 'Start Error Injection' button, and an 'RS-FEC Statistics' section with 'Start Reading RS-FEC Statistics' and 'Reset RS-FEC Statistics' buttons.

| Statistics Counters Names | TX Statistics | RX Statistics |
|-------------------------------------|---------------|---------------|
| Frames < 64 bytes with CRC error | 0 | 0 |
| Oversized frames with CRC error | 0 | 0 |
| Packets with FCS errors | 0 | 0 |
| Frames >= 64 bytes with CRC | 0 | 0 |
| Multicast data frames with CRC | 0 | 0 |
| Broadcast data frames with CRC | 0 | 0 |
| Unicast data frames with CRC | 0 | 0 |
| Multicast control frames with CRC | 0 | 0 |
| Broadcast control frames with CRC | 0 | 0 |
| Unicast control frames with CRC | 0 | 0 |
| Pause frames with CRC error | 0 | 0 |
| 64 Byte Frames (includes CRC field) | 0 | 0 |
| 65 - 127 Byte Frames | 0 | 0 |
| 128 - 255 Byte Frames | 0 | 0 |
| 256 - 511 Byte Frames | 0 | 0 |
| 512 - 1023 Byte Frames | 0 | 0 |
| 1024 - 1518 Byte Frames | 0 | 0 |
| 1519 - MAX Size Frames | 0 | 0 |
| Oversized Frames (> MAX Size) | 0 | 0 |
| Multicast data frames without error | 0 | 0 |

Intel® Advanced Link Analyzer (ALA)

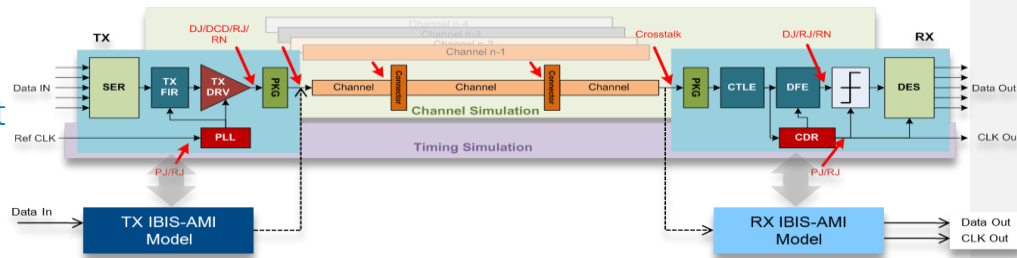
- Advanced HSIO link simulation platform

- IBIS-AMI standard transceiver model support

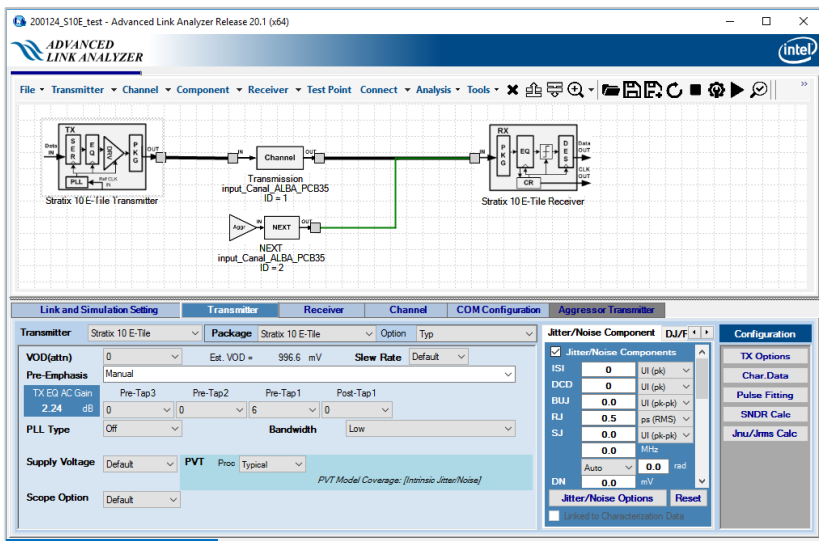
- Intel® and 3rd party devices

- Key Features

- Silicon correlated end-to-end simulation over PVT
- Intel® FPGA family support – IBIS-AMI (Standard and Enhanced w/wrapper) and embedded behavioral models
- Intel® Agilx™ E-Tile, P-Tile, R-Tile, F-Tile (General Purpose and High-Speed Transceiver Blocks)
 - Intel® Stratix® 10 L-Tile/H-Tile/E-Tile/P-Tile, Stratix® V GX/GT, Stratix® IV
 - Intel® Arria® 10 GX/GT, Arria® V GX/GT
 - Intel® Cyclone® 10 GX, Cyclone® V
- Customizable and comprehensive channel modeling and simulation
 - FEC, S-param, COM, ERL, SNDR, Noise Calibration, channel creation, full mixed-mode sim, and others
- Available to Quartus® Prime Standard and Pro Subscription Edition customers



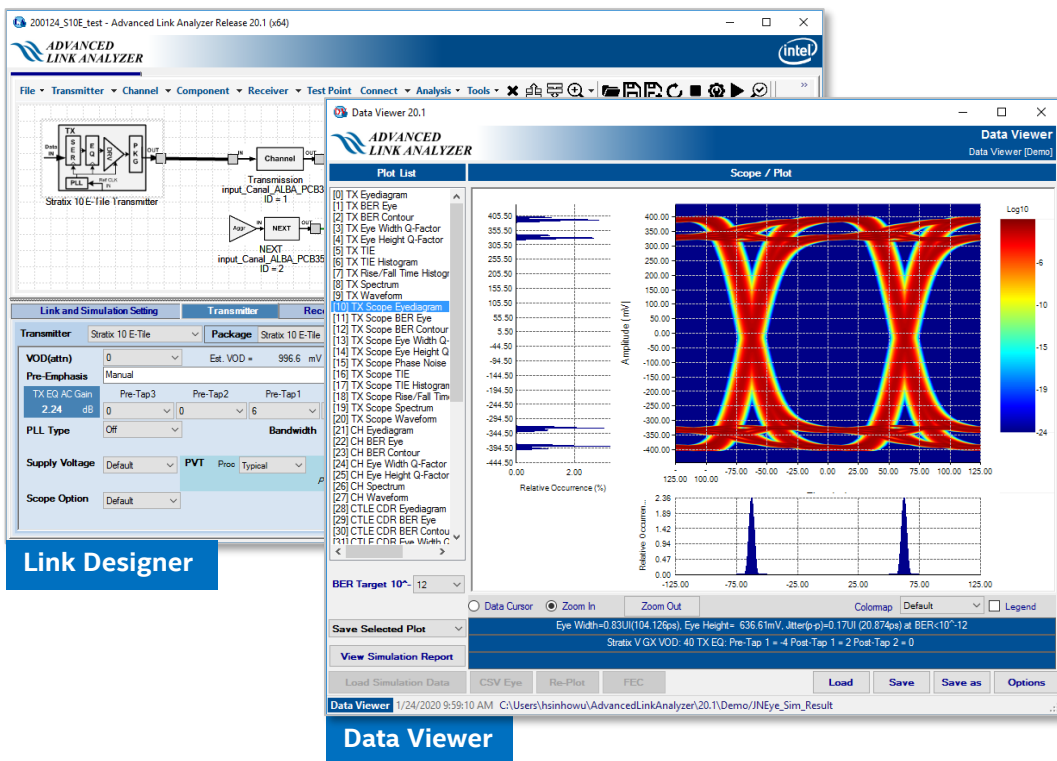
User Interface – ALA Link Simulator



Link Designer

- Ease-of-use and high throughput
- Developed and supported by SI experts
- Standalone tool (can be used w/o Quartus)

User Interface – ALA Link Simulator

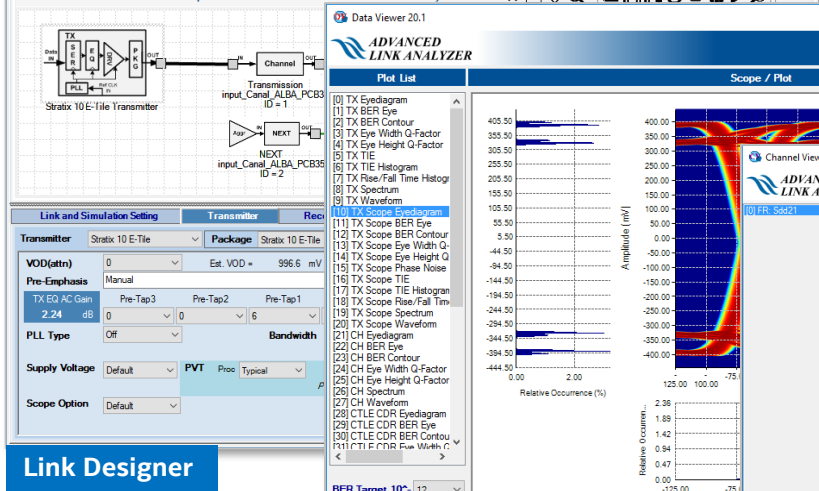
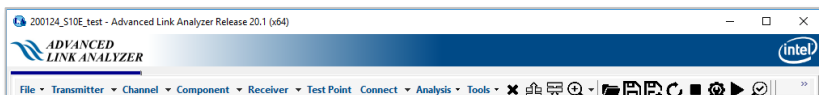


- Ease-of-use and high throughput
- Developed and supported by SI experts
- Standalone tool (can be used w/o Quartus)

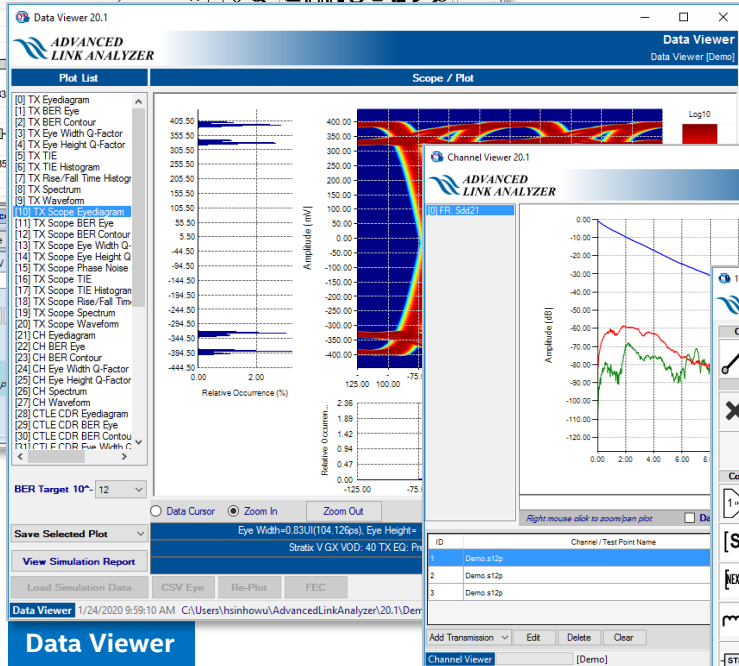


- Ease-of-use and high throughput
- Developed and supported by SI experts
- Standalone tool (can be used w/o Quartus)

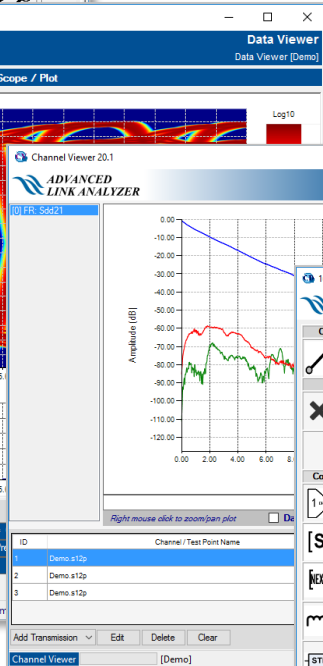
User Interface – ALA Link Simulator



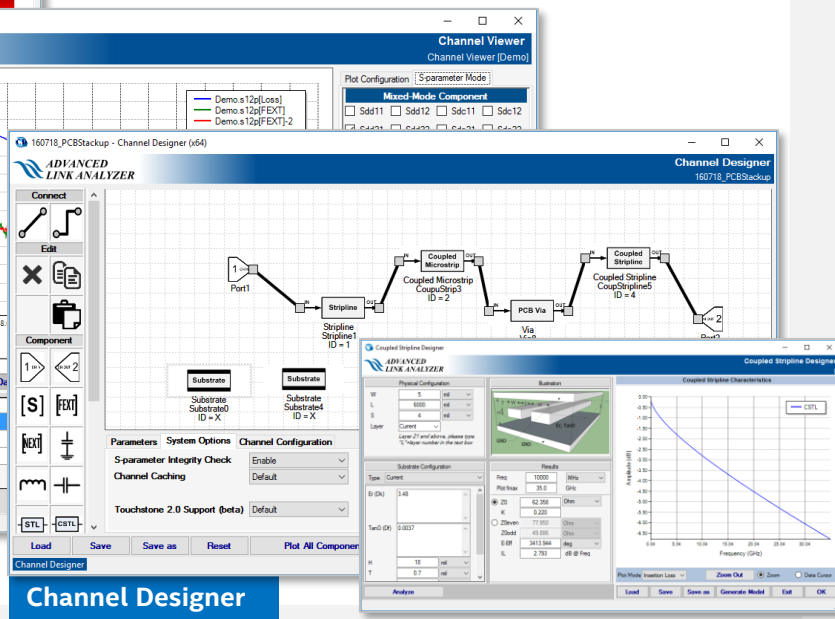
Link Designer



Data Viewer



Channel Viewer



Channel Designer

- Ease-of-use and high throughput
- Developed and supported by SI experts
- Standalone tool (can be used w/o Quartus)

Thank You!

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December 6 - 9, 2021

| Day | Topic |
|-----------------------|--|
| Day 1: Technology | Advances in cloud infrastructure, networking, and computing at edge are accelerating. Flexibility is key to keeping pace with the transforming world. Learn about innovations developed and launched in 2021 along with new Intel FPGA products that address key market transitions. |
| Day 2: Cloud | The cloud is changing. Disaggregation improves data center performance and scalability but requires new tools to keep things optimized. Intel FPGA smart infrastructure enables smarter applications to make the internet go fast. |
| Day 3: Embedded & IoT | As performance and latency continue to dictate compute's migration to the edge, Intel FPGAs provide the workload consolidation and optimization required with software-defined solutions. This is enabled by Intel's vast and growing partner ecosystem. |
| Day 4: Networking | The evolution of 5G continues to push the performance to power envelop, requiring market leaders to adapt or be replaced. Solutions for 5G and beyond will require scalable and programmable portfolios to meet evolving standards and use cases. |

<https://www.intel.com/content/www/us/en/events/fpga/overview.html>

Details on Intel® Agilex™ FPGA Performance, Power and Software Support Numbers

Up to 40% Higher Performance Compared to Intel® Stratix® 10 FPGAs

Derived from benchmarking an example design suite comparing maximum clock speed (Fmax) achieved in Intel® Stratix® 10 devices with the Fmax achieved in Intel® Agilex™ devices, using Intel® Quartus® Prime Software. On average, designs running in the fastest speed grade of Intel® Agilex™ FPGAs achieve a 40% improvement in Fmax compared to the same designs running in the most popular speed grade of Intel® Stratix® 10 devices (-2 speed grade), tested February 2019.

Up to 40% Lower Total Power Compared to Intel® Stratix® 10 FPGAs

Derived from benchmarking an example design suite comparing total power estimates of each design running in Intel® Stratix® 10 FPGAs compared to the total power consumed by the same design running in Intel® Agilex™ FPGAs. Power estimates of Intel® Stratix® 10 FPGA designs are obtained from Intel® Stratix® 10 Early Power Estimator; power estimates for Intel® Agilex™ FPGA designs are obtained using internal Intel® analysis and architecture simulation and modeling, tested February 2019.

Up to 40 TFLOPs of DSP Performance (FP16 Configuration)

Each Intel® Agilex™ DSP block can perform two FP16 floating-point operations (FLOPs) per clock cycle. Total FLOPs for FP16 configuration is derived by multiplying 2x the maximum number of DSP blocks to be offered in a single Intel® Agilex™ FPGA by the maximum clock frequency that will be specified for that block.

30% Improvement in Compile Times / 15% Improvement in Memory Utilization

Comparison is made between Intel® Quartus® Prime Software 18.1 and Intel® Quartus® Prime Software 19.1. Derived from benchmarking an example design suite comparing compile times and memory utilization for designs in Intel® Quartus® Prime Software 18.1 with compile times and memory utilization for same designs in Intel® Quartus® Prime Software 19.1, tested February 2019.

Results have been estimated or simulated using internal Intel® analysis, architecture simulation, and modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.





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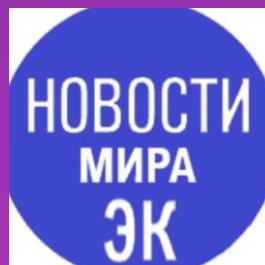
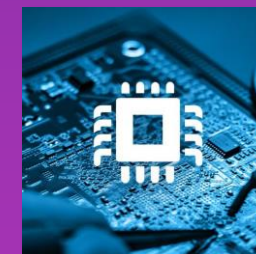
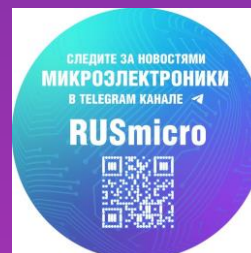


Русская электроника 

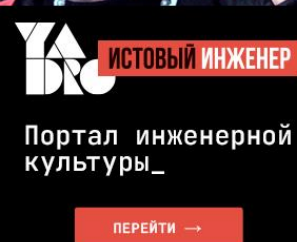


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