III КОНФЕРЕНЦИЯ FPGA РАЗРАБОТЧИКОВ

FPGA-Systems 2021.2

Доступно в записи на Youtube

Конференция в Москве

Конференция в Санкт-Петербурге

Приходи на следующую конференцию

fpga-systems.ru/meet

Поддержи мероприятие

Способ 1

Способ 2

Intel® Agilex™ FPGA Design Seminars

High-Speed Serial Interfaces in Intel® Agilex™ FPGAs

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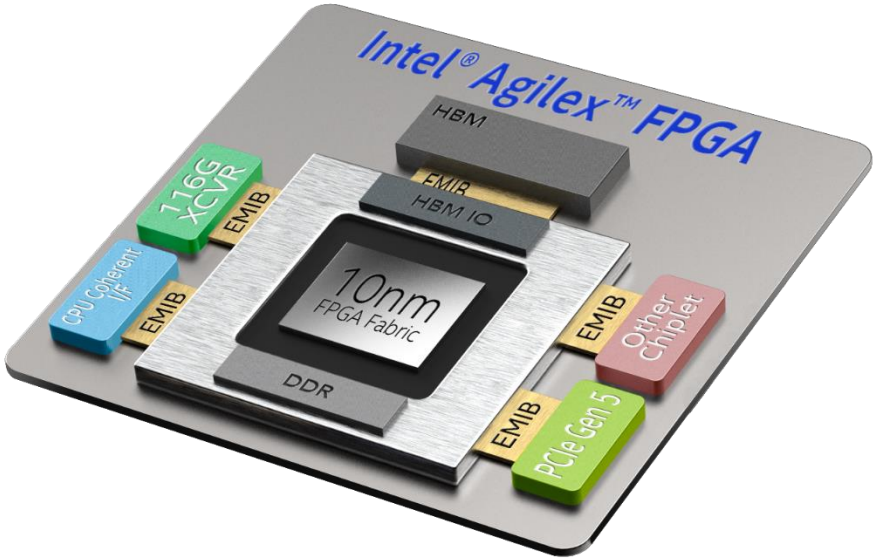
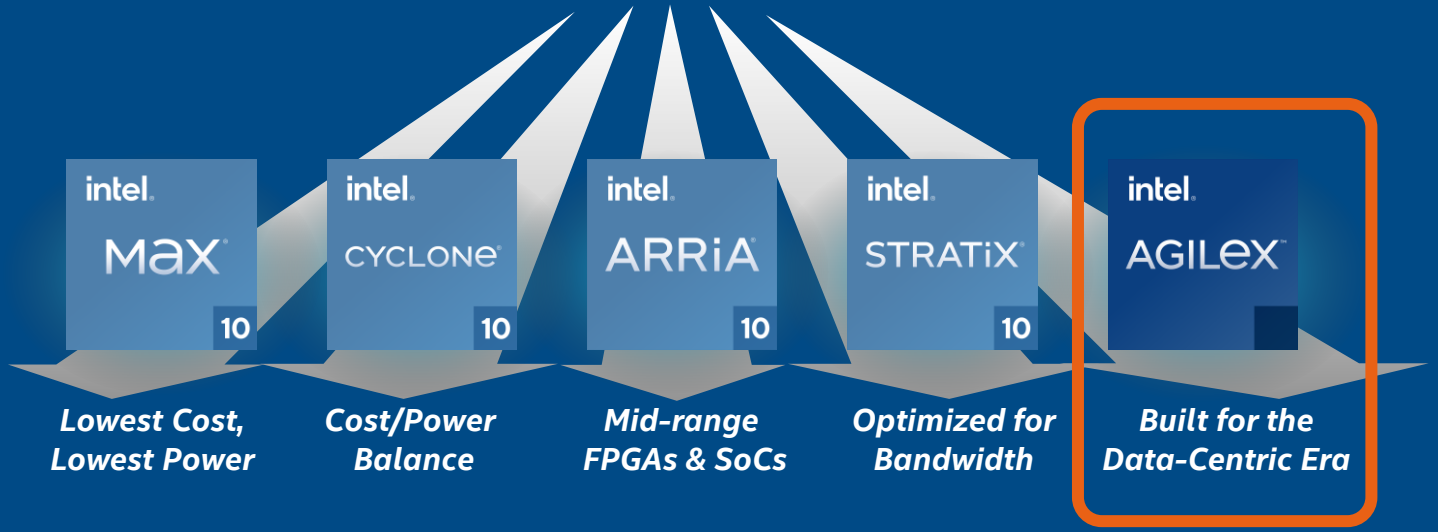
Agenda

- Intel® Agilex Overview
- Transceiver Tiles
- Transceiver Toolkit & Other Tools
- Q&A



Intel® Agilex® Overview

Intel® FPGA Portfolio



Intel® FPGAs and SoC FPGAs for Every Application

The FPGA for the Data-Centric World

Process Data

2nd Generation Intel® Hyperflex ™ Architecture

Up to **40%** Higher [1,3] performance

Up to **40%** Lower [1,3] Power

Up to **40 TFLOPS** DSP Performance [2,3]

Store Data

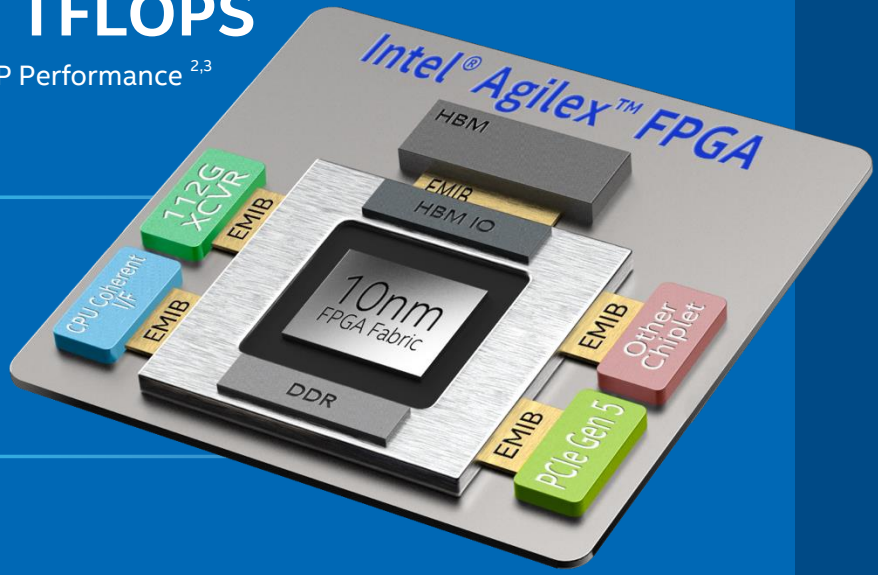
DDR5 SDRAM & High-Bandwidth Memory (HBM) support

Intel® Optane ™ Persistent Memory support

Move Data

Intel® Xeon® Processor coherent connectivity & PCIe* Gen5

116G Transceiver data rates



[1] Compared to Intel® Stratix® 10 FPGAs

[2] With FP16 configuration

[3] Based on current estimates, see backup for details

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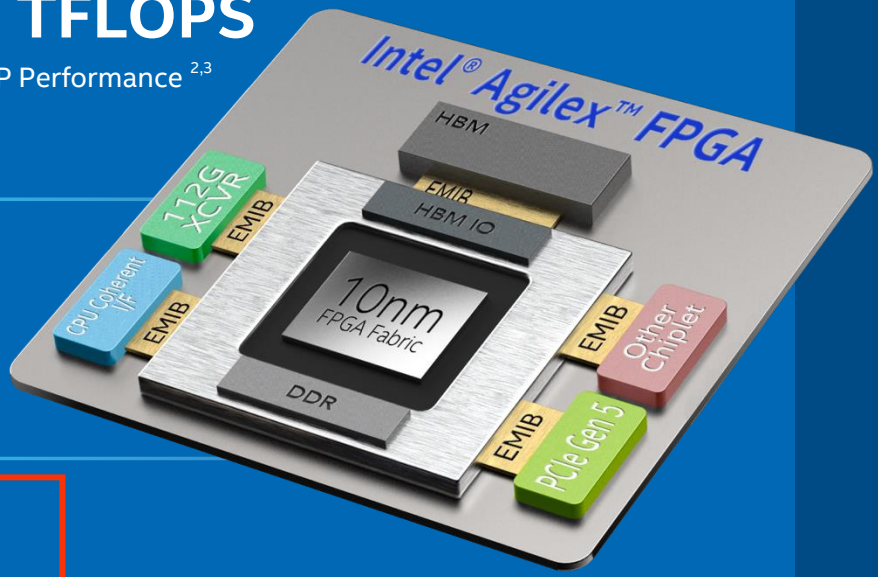

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Intel® EMIB – Enabling Multi-Die Devices

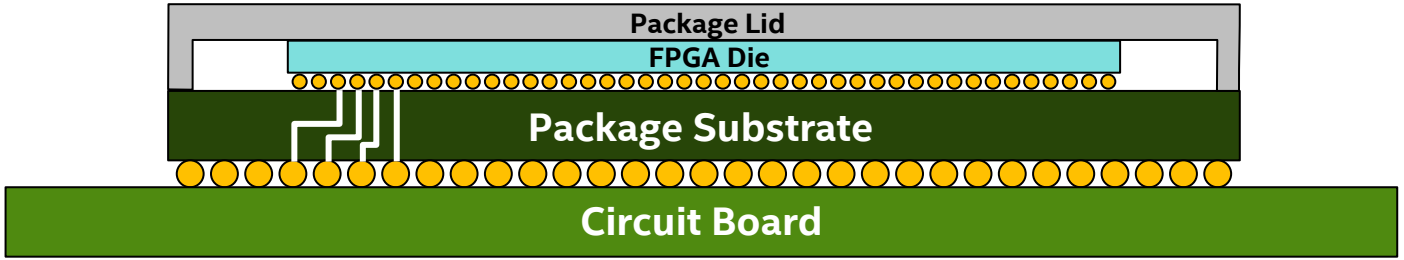


Figure 1. Standard BGA Packaging Technology

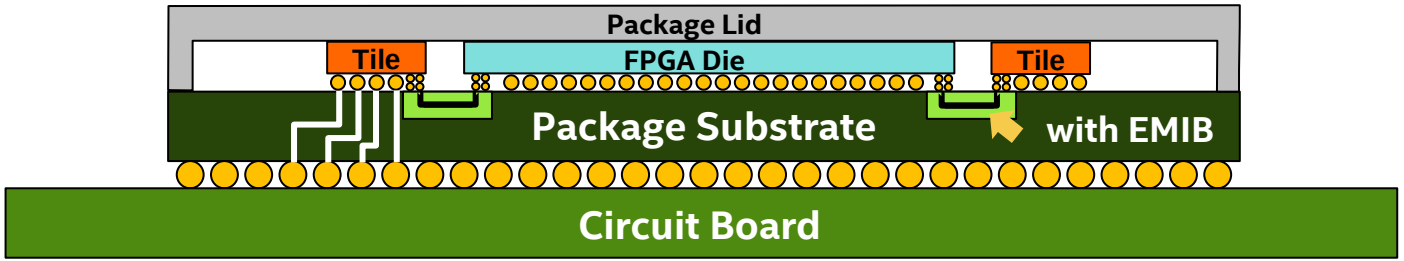
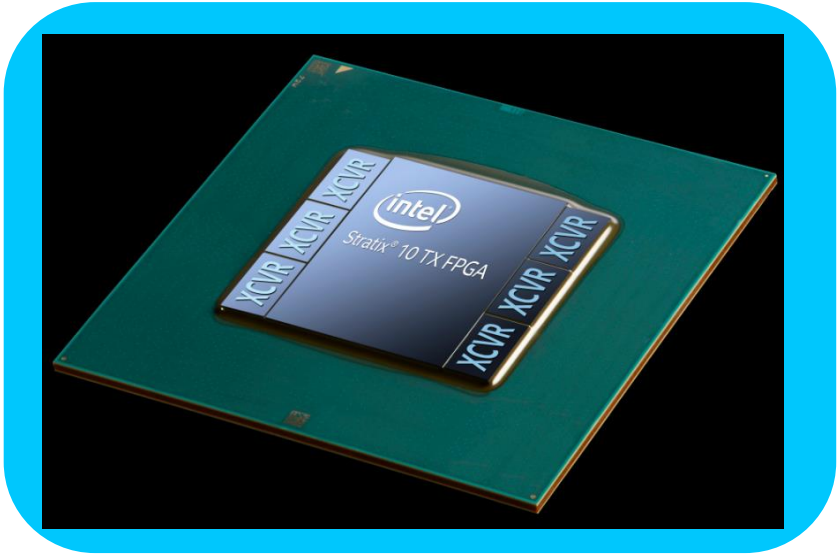
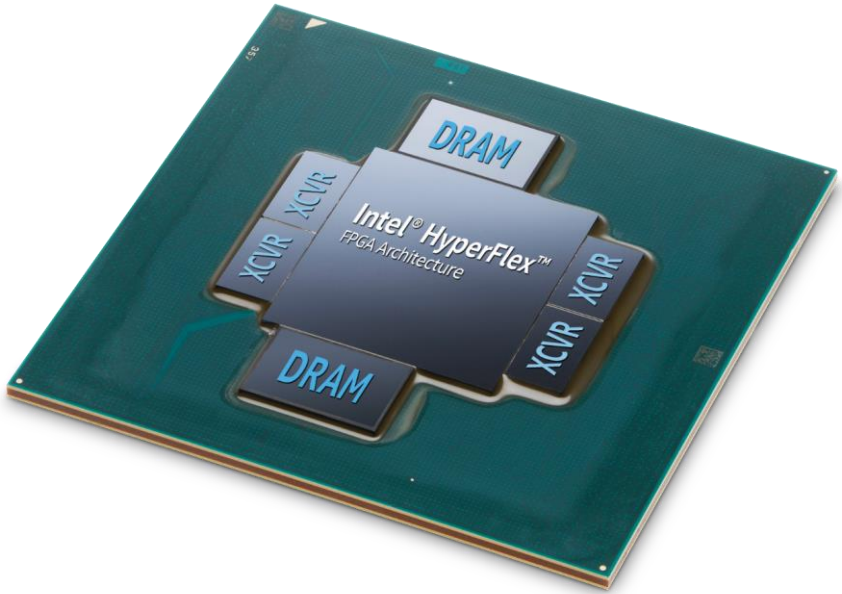


Figure 2. Intel® EMIB (Embedded Multi-Die Interconnect Bridge) Packaging Technology

Intel® Stratix® 10 Devices (Package Lids Removed)



Stratix® 10 TX, E-Tile + H-Tile



Stratix® 10 MX, E-Tile + H-Tile + HBM

Intel® Agilex™ FPGA Family Variants

F - Series

For wide range of applications

- Up to 58Gbps Transceivers
- PCIe Gen 4
- DDR4 Memory Support
- Quad Core Arm* Cortex A53 (optional)

I - Series

For high-performance processor interface and bandwidth-intensive applications

- Coherent attach to Intel® Xeon® Scalable Processor (CXL)
- Up to 116Gbps Transceivers
- PCIe Gen 5
- DDR4 Memory Support
- Quad Core Arm* Cortex A53

M - Series

For compute-intensive applications

- High bandwidth memory (HBM) option
- Coherent attach to Intel® Xeon® Scalable Processor (CXL)
- Up to 116Gbps Transceivers
- PCIe Gen 5
- DDR4, DDR5, Intel® Optane™ Persistent Memory support
- Quad Core Arm* Cortex A53

Transceiver Tiles

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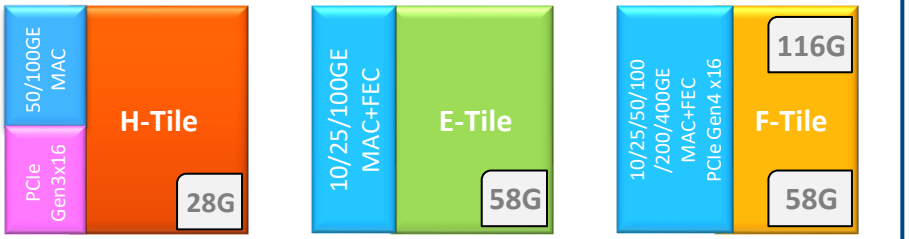
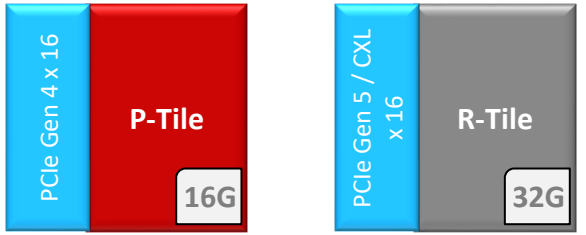
Agilex™ Transceiver Tile Overview

Networking & Communication Tiles

Processor Attach Tiles



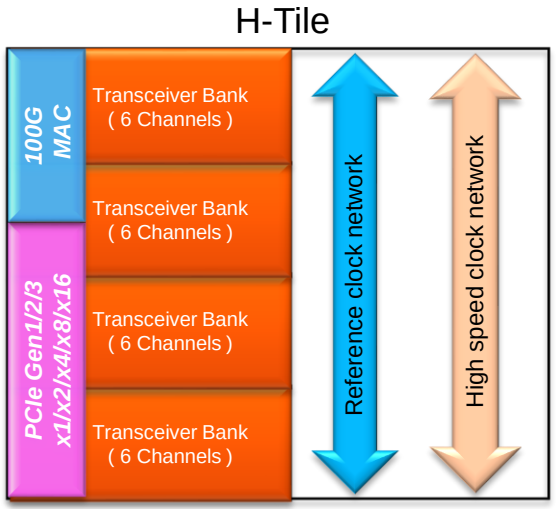


XCVR Tile Options	H-Tile	E-Tile	F-Tile	P-Tile	R-Tile
Maximum Data Rate and Channel Count	16 x 28.3G NRZ or 24 x 17.4G NRZ	12 x 57.8G PAM4 or 24 x 28.9G NRZ	(FHT) 4 x 116G PAM4 plus (FGT) 12 x 58G PAM4 or 16 x 32G NRZ	16 x 16G NRZ	16 x 32G NRZ
Hard IP	PCIe* Gen3 x16 with 4 PF/2K VF SR-IOV 50/100GbE MAC and PCS	10/25/100GbE MAC, PCS and KR/KP RSFEC	PCIe Gen4 x16 EP/RP 8 PF/2K VF SR-IOV 10/25/50/100/200/400Gb E MAC, PCS & KR/KP RSFEC	PCIe Gen4 x16 EP/RP 8 PF/2K VF SR-IOV, VirtIO	PCIe Gen5 x16 EP/RP 8 PF/2K VF SR-IOV, SIOV, SVM, VirtIO CXL v1.1 interface PIPE v5.1.1
	In Production (Stratix® 10)	In Production (Stratix® 10)	New for Intel® Agilex™ FPGAs	In Production (Stratix® 10)	New for Intel® Agilex™ FPGAs

H-Tile Architecture

- H-Tile contains all analog and digital circuits to develop high speed data interfaces
  - 24 transceiver channels
  - PLLs
  - Clock networks
  - Hard IP blocks
    - 1x PCIe Gen3 (w/SR-IOV)
      - 4 Physical Functions, 2K Virtual Functions
    - 1x100G Ethernet
      - 100 GbE MAC

Feature	H-Tile
Total Transceivers	24 per tile
Max Chip-to-Chip	28.3G NRZ
# at Max Rate	16 @ 28.3G + 8 @ 17.4G
Max Backplane	28.3G up to 30 dB



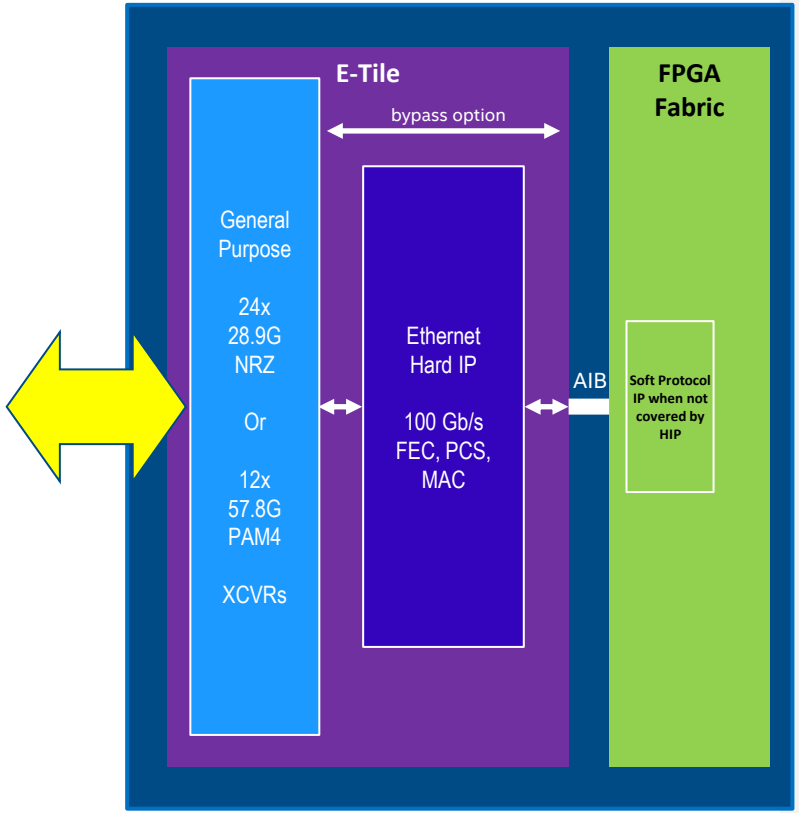
E-Tile Architecture

General Purpose

- 24 XCVR channels @ 28.9Gbps NRZ
  or
  12 XCVR channels @ 57.8Gbps PAM4
- Multi-protocol support for CEI, Ethernet, CPRI, FlexE, Interlaken, Fibre Channel, SRIO, Serial Lite, OTN, JESD204B/C, FlexO

Networking: 100 GbE

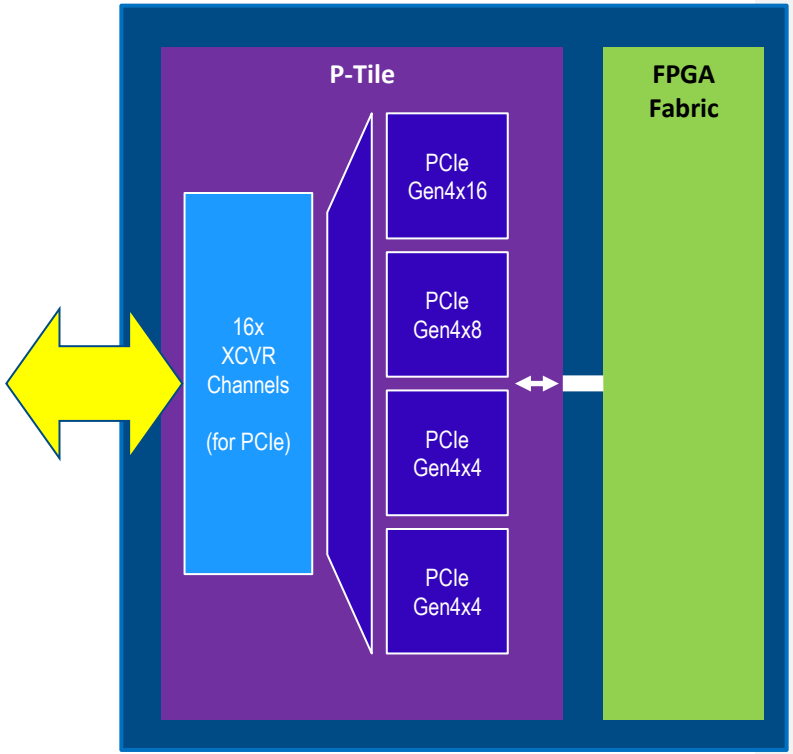
- 24 x 10/25 GbE FEC/PCS/MAC
- 4 x 100 GbE FEC/PCS/MAC
  - 6x RS-FEC
  - 6x KP-FEC(1)
- IEEE 1588 support (Precision Time Protocol)



(1) Only 4 instances of KP-FEC are supported when using 100GbE MAC

P-Tile Architecture

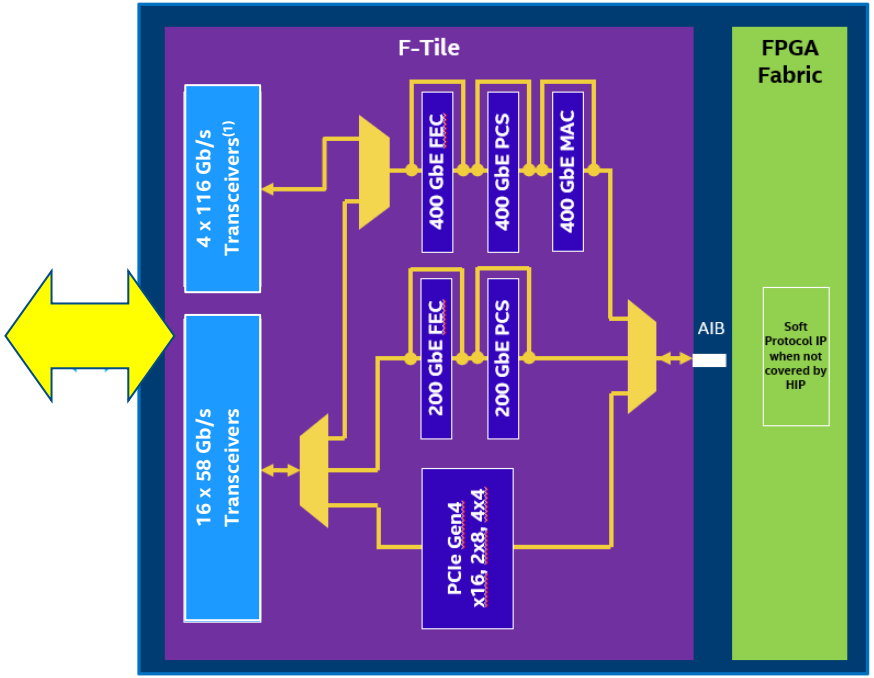
- PCIe Gen4 x16 – 2x bandwidth versus H-Tile
  - PCIe Gen4 x16-lanes up to 16 GT/s (End Point or Root Port)
    - Port Bifurcation support: 2x8 (EP only) or 4x4 (RP only)
    - Optimized for lower latency & higher performance
  - Enhanced Virtualization
    - SR-IOV supporting 8 PFs/2048 VFs
- CvP Initialization, Autonomous HIP
- VirtIO support
- Scalable IOV
- Shared Virtual Memory



Generic protocols and hard IP bypass NOT supported on P-tile

F-Tile Architecture

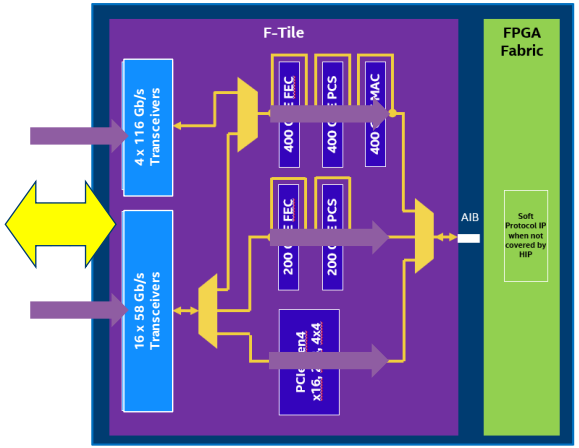
- XCVR Support
  - High-Speed XCVRs
  - FHT: 4 channels 96-116Gbps PAM4(1)
    - Or 48-58Gbps NRZ/PAM4 or 24-29Gbps NRZ
  - FGT: General Purpose XCVRs
    - 16 channels 1-32Gbps NRZ
    - or 12 channels 20-58Gbps PAM4
  - PMA Direct Mode
- PCIe Gen4 x16
  - P-Tile feature set plus:
    - Precise Time Management
- Advanced Networking Support: 400 GbE
  - IEEE 1588 support
  - 10/25/50/100/200/400 GbE FEC/PCS/MAC
  - 600G Interlaken
- General Purpose
  - Multi-protocol support for CEI, Ethernet, CPRI, JESD204B/C, FlexE, Interlaken, Fibre Channel, InfiniBand, SRIO, Serial Lite, PCIe, GPON, FlexO, SDI, OTN, HDMI, DisplayPort



(1) Not supported in Agilex™ F-series devices

F-Tile Topologies

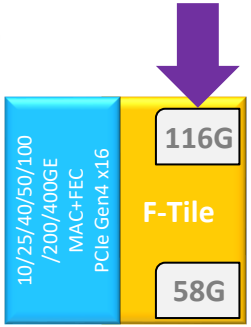
- F-Tile supports 15 defined system level topologies across:
  - Three separate bifurcatable datapath's, 400G, 200G & PCIe paths
  - Two XCVR blocks, High Speed (FHT), 116Gbps and General Purpose (FGT), 58Gbps sources



(1) I-Series devices only

	Supported Datapath Configuration					
	400G DataPath		200G DataPath		PCIe Datapath	
#	XCVR	Mode	XCVR	Mode	XCVR	Mode
0	*n/a*	Disabled	*n/a*	Disabled	*n/a*	Disabled
1	*n/a*	Disabled	*n/a*	Disabled	FGT	PCIe Gen4 x16
2	*n/a*	Disabled	*n/a*	Disabled	FGT	2x PCIe Gen4 x8
3	FHT(1)	100G-4 w/PTP	*n/a*	Disabled	FGT	PCIe Gen4 x16
4	*n/a*	Disabled	*n/a*	Disabled	FGT	4x PCIe Gen4 x4
5	FHT(1)	400G-4	GP	200G-8	*n/a*	Disabled
6	FHT(1)	400G-4 w/PTP	GP	150G-6	*n/a*	Disabled
7	FHT(1)	400G-4 w/PTP	*n/a*	Disabled	FGT	PCIe Gen4 x4
8	FHT(1)	250G-4 w/PTP	*n/a*	Disabled	FGT	PCIe Gen4 x8
9	FHT(1)	250G-4 w/PTP	*n/a*	Disabled	FGT	2x PCIe Gen4 x4
10	FGT	400G-8	GP	200G-8	*n/a*	Disabled
11	FGT	400G-8 w/PTP	GP	150G-6	*n/a*	Disabled
12	FGT	275G-8 w/PTP	*n/a*	Disabled	FGT	PCIe Gen4 x8
13	FGT	275G-8 w/PTP	*n/a*	Disabled	FGT	2x PCIe Gen4 x4
14	FGT	400G-12 w/PTP	*n/a*	Disabled	FGT	PCIe Gen4 x4
15	FGT	400G-16 w/PTP	*n/a*	Disabled	*n/a*	Disabled

Supported Standards and Protocols – FHT

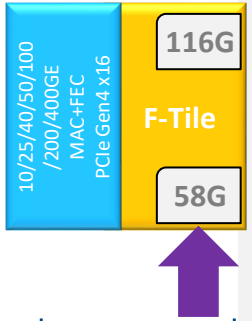


- All 4 High-Speed Transceivers (FHT) independent of each other
- Support Ethernet and CEI standards
- Feeds into 400G Hard IP block for Ethernet & CEI

Supported Standards & Protocols
CEI: 112G PAM4-LR/MR/SR, 56G NRZ/PAM4-XSR, 56G NRZ-USR, 56G PAM4-LR/MR/SR/VSR, 25G-LR, 28G MR/VSR
Ethernet (IEEE802.3): 25GbE/50GbE/200GbE/400GbE
SerialLite IV, Interlaken, FlexE, OTN

CEI – Common Electrical I/O

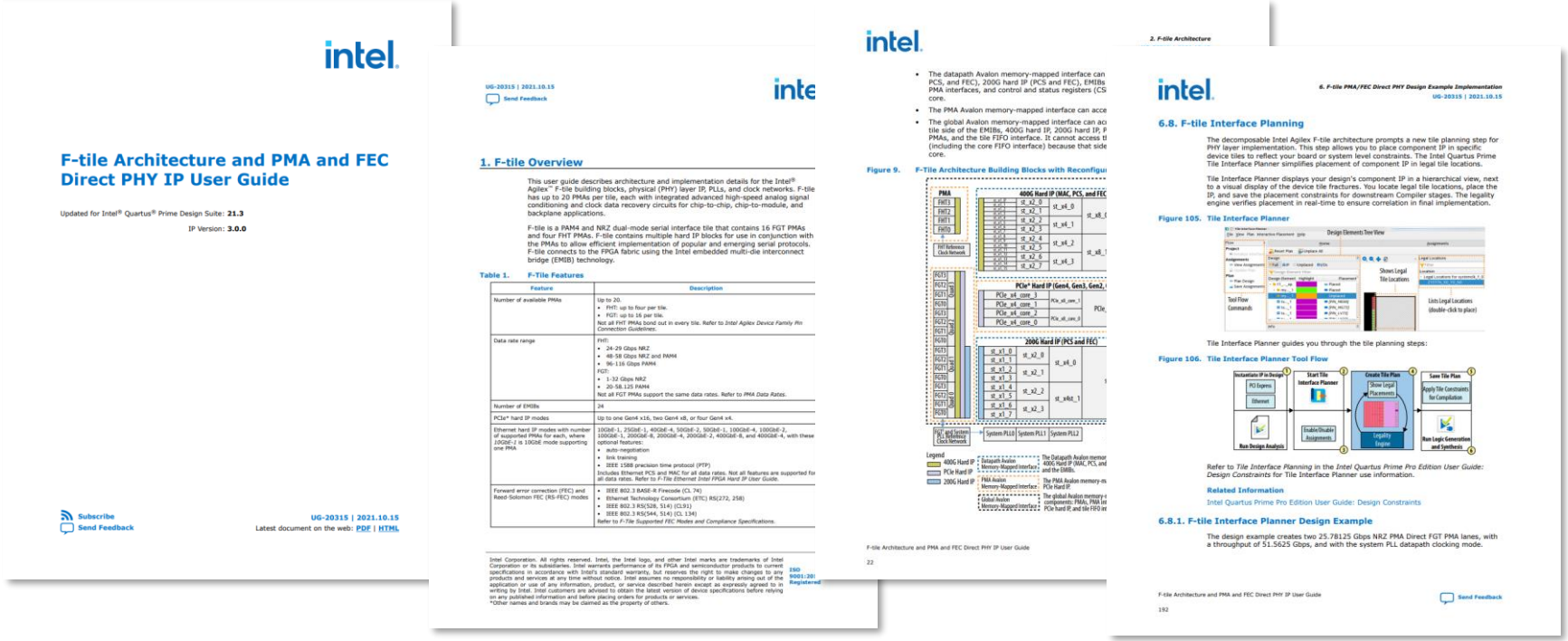
Supported Standards and Protocols – FGT



- All 16 General-Purpose Transceivers independent of each other
- Support many standards and protocols
- Feeds into 200G and 400G Hard IP block, and PCIe block
- Does NOT feed 400G Hard IP block with High-Speed SERDES simultaneously

Supported Standards & Protocols
CEI: 56G PAM4-LR/MR/SR/VSR, 25G-LR, 28G MR/VSR, 11G LR/MR/SR/VSR; 6G LR/SR
Ethernet (IEEE802.3): 10GbE/25GbE/40GbE/50GbE/100GbE/200GbE/400GbE
PCIe Gen1/Gen2/Gen3/Gen4
CPRI, SFF 8431/8418/8402, OTL, OTU, OTN
JESD204B/C, SerialLite IV, FlexE, FlexO
DisplayPort, HDMI, SDI
Interlaken, GPON/EPON, FibreChannel,
SAS, SATA, USB 3.1, V-by-One

F-Tile Documentation

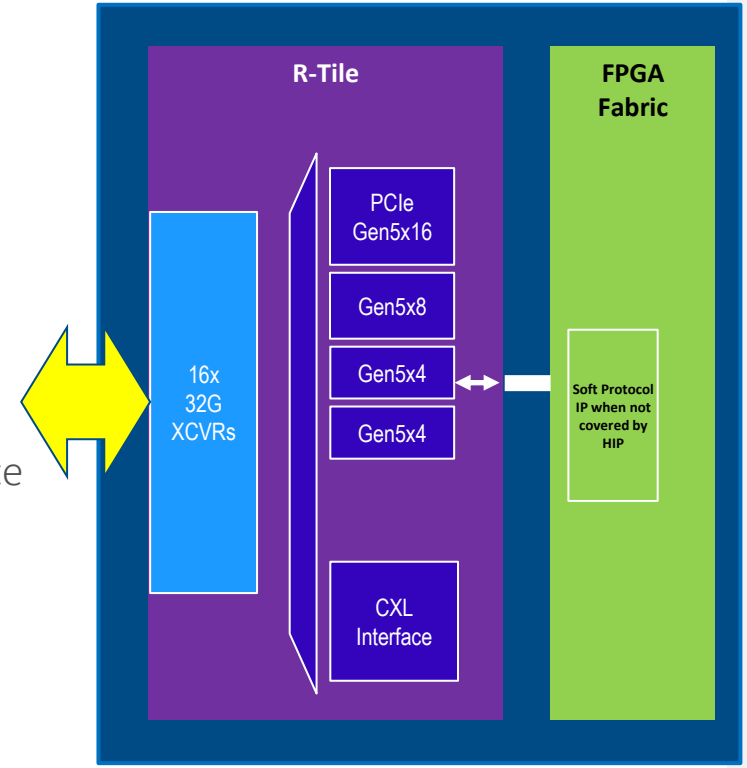


https://www.intel.com/content/www/us/en/products/details/fpga/intellectual-property/interface-protocols/agilex-f-tile-hard-ip.html
https://www.intel.com/content/www/us/en/programmable/documentation/qty1599073551174.html

R-Tile Architecture

- Compute Express Link (CXL)
  - Low latency, coherency for high-performance acceleration
- PCIe Gen5 x16-lanes up to 32G (EP or RP)
  - Port Bifurcation support: 2x8 EP or 4x4 RP
- CvP Initialization, Autonomous HIP
- Separate header and payload interfaces on user interface
- Virtualization (SR-IOV) supporting 8 PFs/2k VFs
- Scalable IOV
- Shared virtual memory
- VirtIO Support
- Precise Time Management
- PMA PIPE

Preliminary and subject to change



R-Tile can be configured to operate in either PCIe ***OR*** CXL mode, but not both simultaneously

Transceiver Toolkit & Other Tools

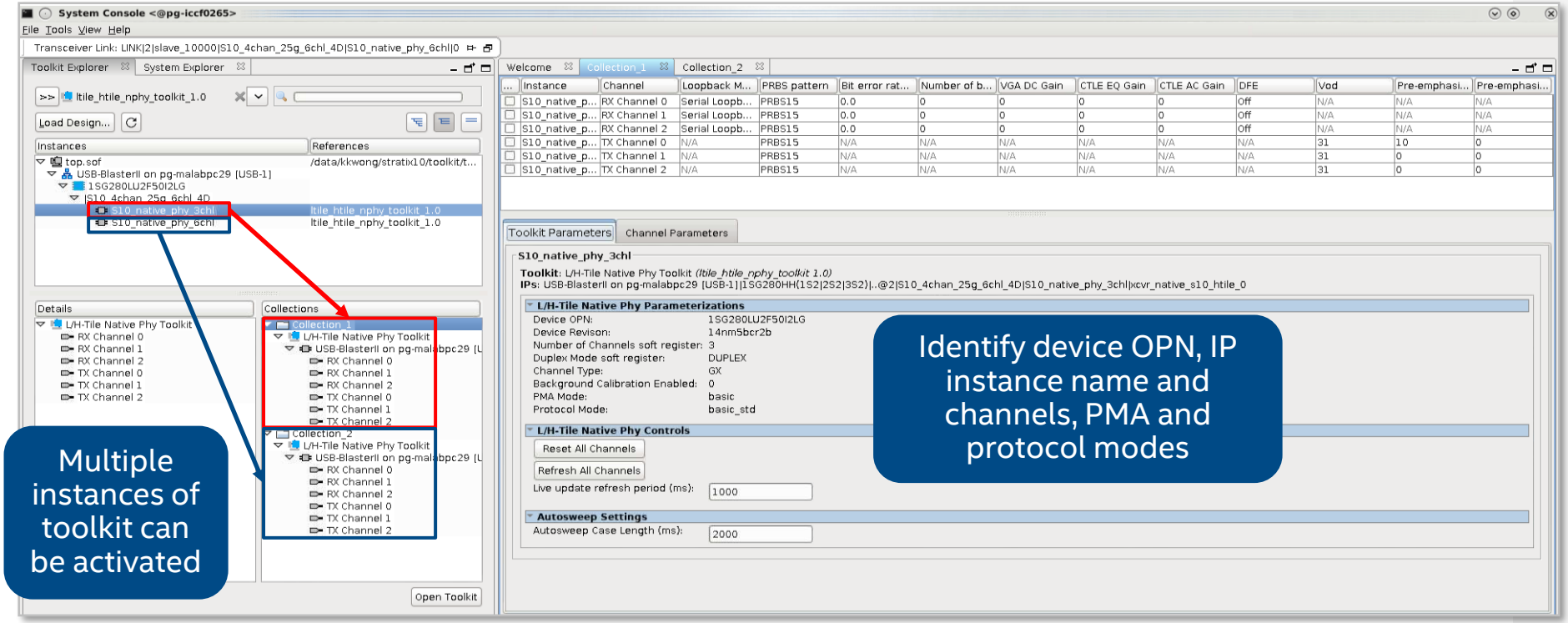
intel®

Transceiver Toolkit Overview

The Transceiver Toolkit (TTK) is a powerful analog verification tool

- Quickly analyzes the transceiver signal quality and performance
- Generates and checks pseudo-random binary sequence (PRBS) patterns to measure the BER
- Dynamically changes transceiver buffer settings under automatic or manual control
- Creates eye diagrams at RX for NRZ and PAM4 modulation
- Supports a variety of design situations
- Comes free with any licensed version of the Intel® Quartus® Prime software

Transceiver Toolkit GUI



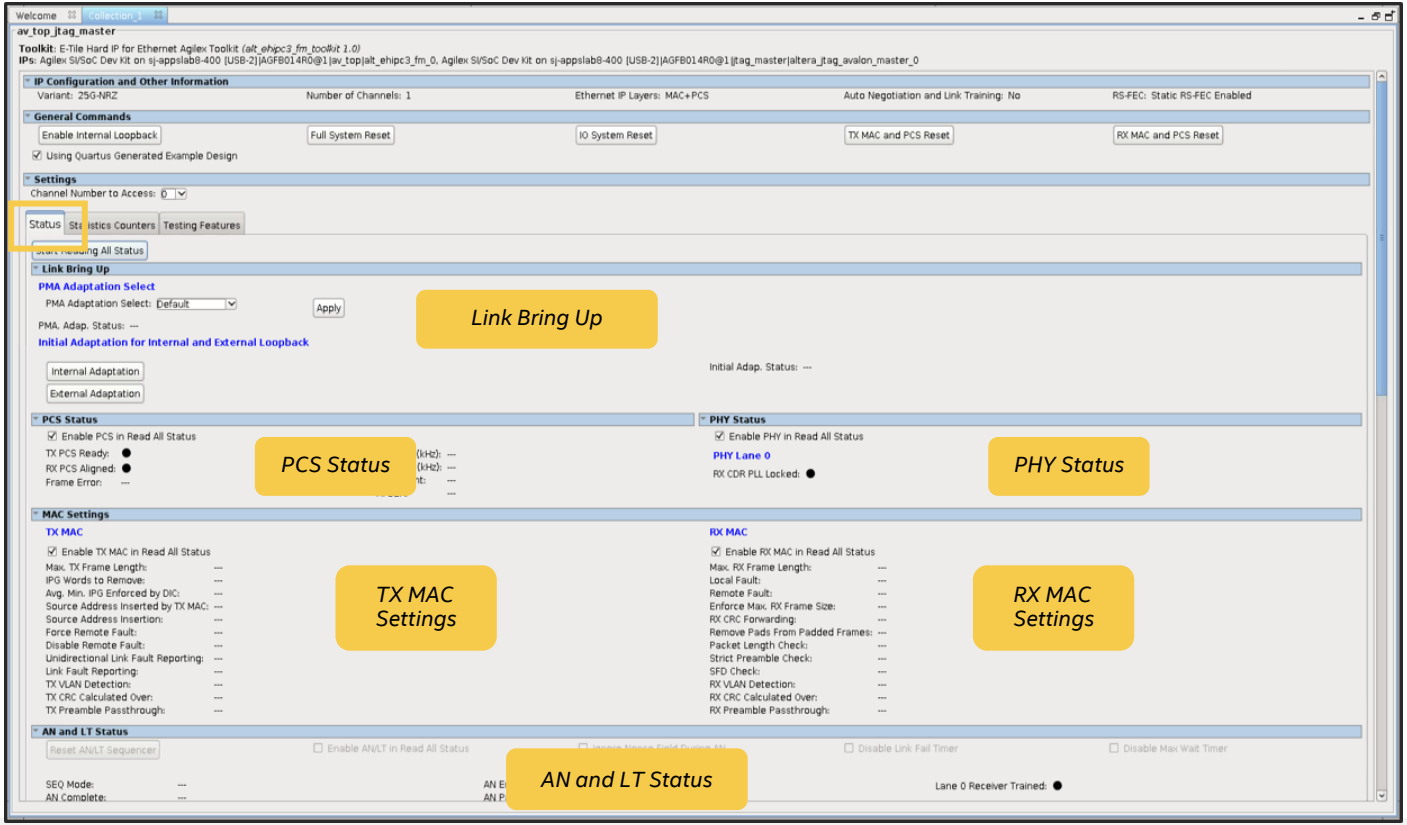
Ethernet Toolkit

- The Ethernet Toolkit is Intel® FPGA on-chip debugging tool for analyzing real-time status of Ethernet Intel FPGA IP

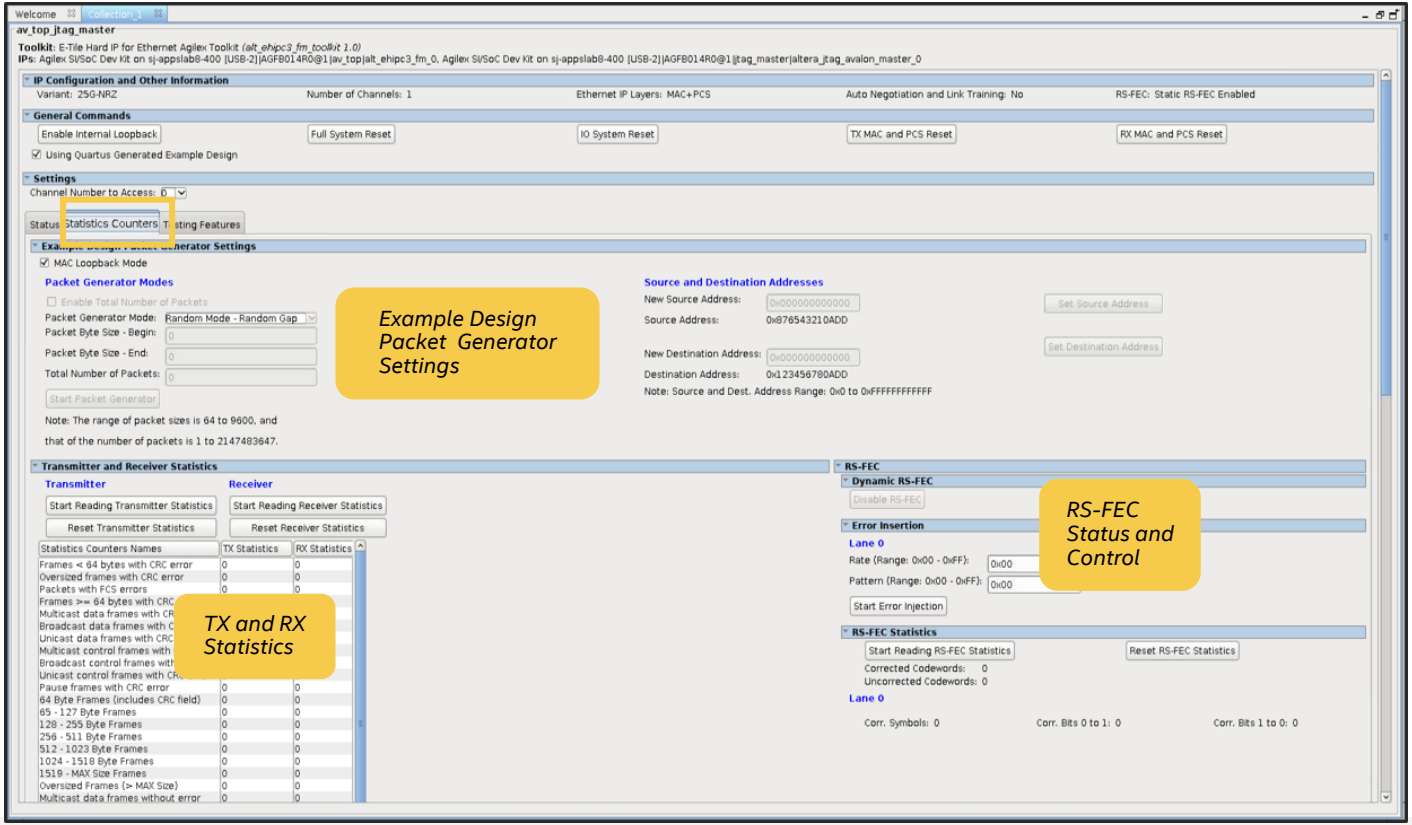
- Runs on System Console platform
- Interfaces with Ethernet IP through FPGA's JTAG connection
- Continuously monitors IP functions through its registers
- Provides graphical interface for accessing Ethernet IP and link information

** For more details on using the System Console, see the online training entitled System Console*

Ethernet Toolkit: Status Tab

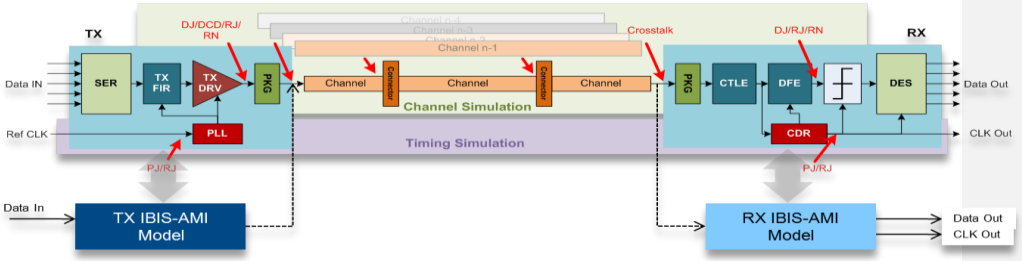


Ethernet Toolkit: Statistics Counters Tab

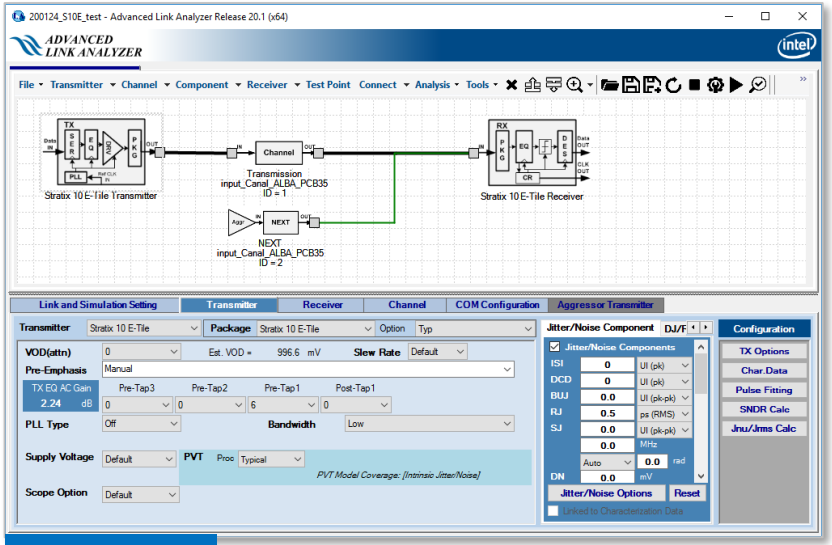


Intel® Advanced Link Analyzer (ALA)

- Advanced HSIO link simulation platform
- IBIS-AMI standard transceiver model support
  - Intel® and 3rd party devices
- Key Features
  - Silicon correlated end-to-end simulation over PVT
  - Intel® FPGA family support – IBIS-AMI (Standard and Enhanced w/wrapper) and embedded behavioral models
    - Intel® Agilex™ E-Tile, P-Tile, R-Tile, F-Tile (General Purpose and High-Speed Transceiver Blocks)
    - Intel® Stratix® 10 L-Tile/H-Tile/E-Tile/P-Tile, Stratix® V GX/GT, Stratix® IV
    - Intel® Arria® 10 GX/GT, Arria® V GX/GT
    - Intel® Cyclone® 10 GX, Cyclone® V
  - Customizable and comprehensive channel modeling and simulation
    - FEC, S-param, COM, ERL, SNDR, Noise Calibration, channel creation, full mixed-mode sim, and others
  - Available to Quartus® Prime Standard and Pro Subscription Edition customers



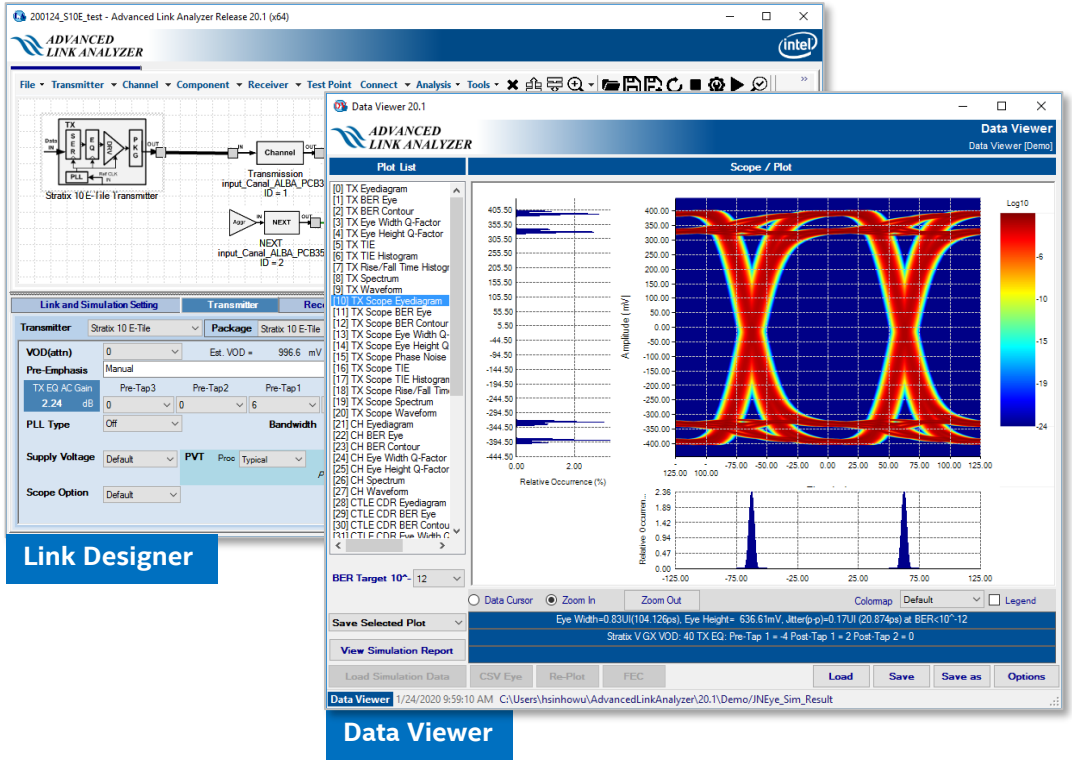
User Interface – ALA Link Simulator



Link Designer

- **Ease-of-use and high throughput**
- **Developed and supported by SI experts**
- **Standalone tool (can be used w/o Quartus)**

User Interface – ALA Link Simulator



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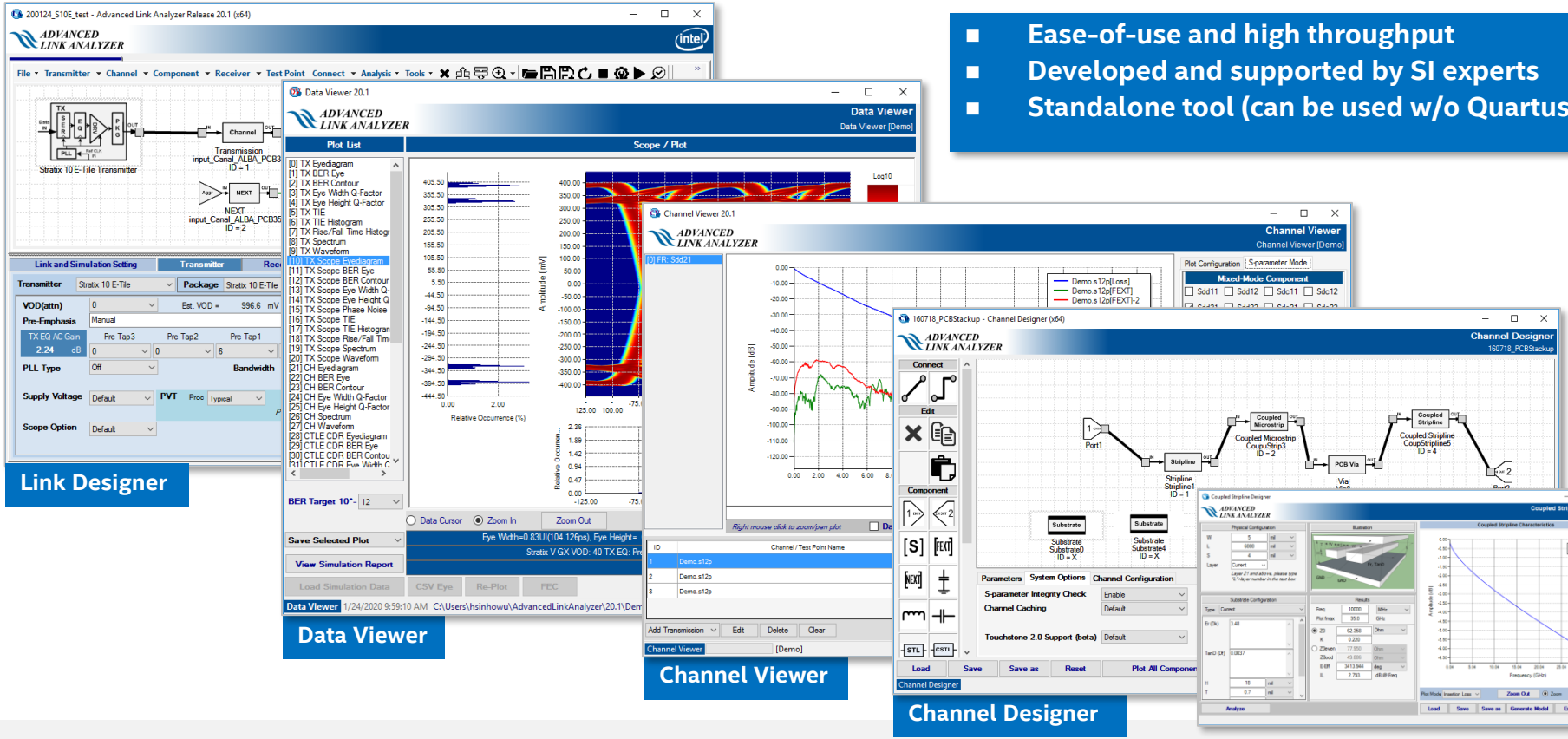
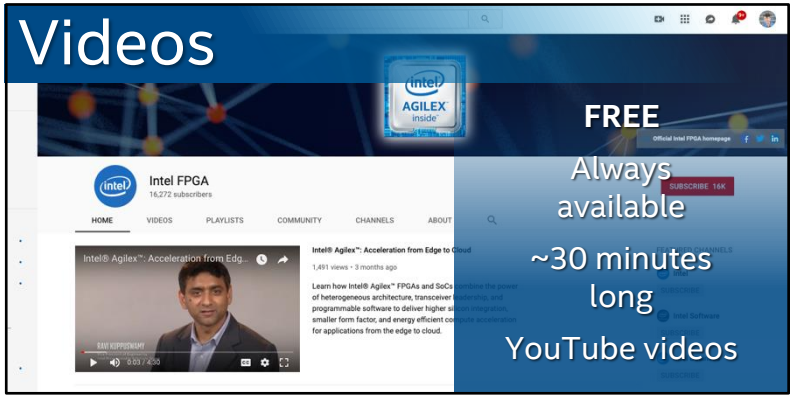


Thank You!

Many Ways to Learn

Videos



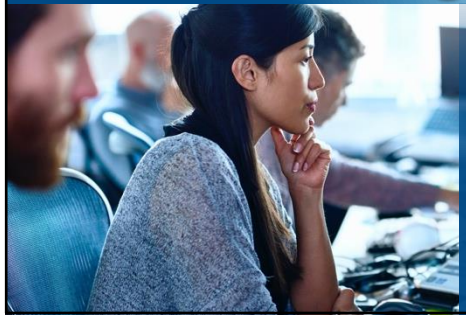
FREE

Always available

~30 minutes long

YouTube videos

Online Training



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Hands on labs

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Intel® FPGA Technology Day

December 6 - 9, 2021

Day	Topic
Day 1: Technology	Advances in cloud infrastructure, networking, and computing at edge are accelerating. Flexibility is key to keeping pace with the transforming world. Learn about innovations developed and launched in 2021 along with new Intel FPGA products that address key market transitions.
Day 2: Cloud	The cloud is changing. Disaggregation improves data center performance and scalability but requires new tools to keep things optimized. Intel FPGA smart infrastructure enables smarter applications to make the internet go fast.
Day 3: Embedded & IoT	As performance and latency continue to dictate compute's migration to the edge, Intel FPGAs provide the workload consolidation and optimization required with software-defined solutions. This is enabled by Intel's vast and growing partner ecosystem.
Day 4: Networking	The evolution of 5G continues to push the performance to power envelop, requiring market leaders to adapt or be replaced. Solutions for 5G and beyond will require scalable and programmable portfolios to meet evolving standards and use cases.

https://www.intel.com/content/www/us/en/events/fpga/overview.html

Details on Intel® Agilex™ FPGA Performance, Power and Software Support Numbers

Up to 40% Higher Performance Compared to Intel® Stratix® 10 FPGAs

Derived from benchmarking an example design suite comparing maximum clock speed (Fmax) achieved in Intel® Stratix® 10 devices with the Fmax achieved in Intel® Agilex™ devices, using Intel® Quartus® Prime Software. On average, designs running in the fastest speed grade of Intel® Agilex™ FPGAs achieve a 40% improvement in Fmax compared to the same designs running in the most popular speed grade of Intel® Stratix® 10 devices (-2 speed grade), tested February 2019.

Up to 40% Lower Total Power Compared to Intel® Stratix® 10 FPGAs

Derived from benchmarking an example design suite comparing total power estimates of each design running in Intel® Stratix® 10 FPGAs compared to the total power consumed by the same design running in Intel® Agilex™ FPGAs. Power estimates of Intel® Stratix® 10 FPGA designs are obtained from Intel® Stratix® 10 Early Power Estimator; power estimates for Intel® Agilex™ FPGA designs are obtained using internal Intel® analysis and architecture simulation and modeling, tested February 2019.

Up to 40 TFLOPs of DSP Performance (FP16 Configuration)

Each Intel® Agilex™ DSP block can perform two FP16 floating-point operations (FLOPs) per clock cycle. Total FLOPs for FP16 configuration is derived by multiplying 2x the maximum number of DSP blocks to be offered in a single Intel® Agilex™ FPGA by the maximum clock frequency that will be specified for that block.

30% Improvement in Compile Times / 15% Improvement in Memory Utilization

Comparison is made between Intel® Quartus® Prime Software 18.1 and Intel® Quartus® Prime Software 19.1. Derived from benchmarking an example design suite comparing compile times and memory utilization for designs in Intel® Quartus® Prime Software 18.1 with compile times and memory utilization for same designs in Intel® Quartus® Prime Software 19.1, tested February 2019.

Results have been estimated or simulated using internal Intel® analysis, architecture simulation, and modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.


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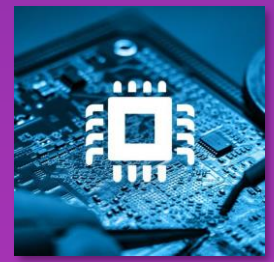

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